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Nonlinear Ion Dynamics Enable Spike Timing Dependent Plasticity of Electrochemical Ionic Synapses

*Mantao Huang, Longlong Xu, Jesús A. del Alamo, Ju Li, and Bilge Yildiz**

Programmable synaptic devices that can achieve timing-dependent weight updates are key components to implementing energy-efficient spiking neural networks (SNNs). Electrochemical ionic synapses (EIS) enable the programming of weight updates with very low energy consumption and low variability. Here, the strongly nonlinear kinetics of EIS, arising from nonlinear dynamics of ions and charge transfer reactions in solids, are leveraged to implement various forms of spike-timing-dependent plasticity (STDP). In particular, protons are used as the working ion. Different forms of the STDP function are deterministically predicted and emulated by a linear superposition of appropriately designed pre- and post-synaptic neuron signals. Heterogeneous STDP is also demonstrated within the array to capture different learning rules in the same system. STDP timescales are controllable, ranging from milliseconds to nanoseconds. The STDP resulting from EIS has lower variability than other hardware STDP implementations, due to the deterministic and uniform insertion of charge in the tunable channel material. The results indicate that the ion and charge transfer dynamics in EIS can enable bio-plausible synapses for SNN hardware with high energy efficiency, reliability, and throughput.

1. Introduction

Artificial neural networks have shown promising applications in a wide range of fields including image and speech recognition, natural language processing, and content generation.[1–3] However, such computations are becoming prohibitively energy-intensive to perform on conventional digital computers.[4–6] Human brains function with spiking signals from billions of neurons with trillions of synaptic connections, at a power consumption of only tens of watts.[7] Inspired by the energy-efficient spike-based biological systems, spiking neural networks (SNNs) have the potential to realize substantial enhancements in the energy efficiency of computing. SNNs are spike-driven networks that use sparse and asynchronous spiking events and biologically realistic behavior of synapses and neurons for carrying out computations.[8–11] These systems are adaptive, as they can perform online learning to adapt to new situations over time, while traditional neural networks need to be trained with back-propagation in separate cycles. SNNs can implement local learning rules, taking input from pre- and post-synaptic neurons, offering the potential for powering low-energy smart devices with adaptive sensory processing[12] and real-time learning.[13] Artificial spiking neurons have also shown promise to interface with biochemical signals by leveraging ion-based operating mechanisms in organic materials.[14–16]

One of the key components to implementing SNN hardware is the synaptic device that has to emulate timing-dependent learning rules, such as spike-timing-dependent plasticity (STDP). STDP is an important learning rule in brain synapses.[17] Emulating STDP serves as a basis for further explorations to achieve more bio-realistic and more capable machine intelligence beyond traditional deep neural networks.[9] STDP learning rules essentially strengthen or weaken the synaptic connection between two neurons when the spiking events of the pre-and post-synaptic neuron take place in a specific temporal sequence.[18] The synaptic weight change, or conductance change, ΔG, is a function of the relative timing, Δt, of the spiking events, and such a function is called the STDP function. One common form of STDP is that the synaptic weight change is positive if the post-neuron fires shortly after the pre-neuron, and negative if the pre-neuron fires shortly after the post-neuron. The modulation strength in this form of STDP increases when the pre-and post-synaptic neurons fire close to each other, and the magnitude decreases with increasing Δt between the two firing events. STDP has been shown to enable coincidence detection,[19] latency reduction,[20] and

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supervised and unsupervised learning.[21] STDP has remarkable diversity in the sign, symmetry, and shape of plasticity.[18] Heterogeneous STDP functions are also observed to occur in the same brain region, even at synapses from the same pre-synaptic neurons connecting to different post-synaptic neuron types.[22,23] For example, in the dorsal cochlear nucleus, synapses that connect the parallel fiber to fusiform cells follow different synaptic plasticity rules compared to the synapses that connect the same parallel fiber to the cartwheel cells.[22] Such diversity and versatility of biologically observed STDP require the hardware platform to have the same flexibility to implement these different STDP forms.

Programmable resistors based on conductive filament formation,[19,24–27] phase-change mechanism,[28,29] and ferroelectricity[30–32] have been explored to implement time-dependent update rules such as STDP for SNN hardware. The stochasticity of the conducting filament-forming process causes high variability in conductance updates and unreliability of training.[33] The phase-change mechanism has been associated with high energy consumption and conductance drift.[33,34] Ferroelectric tunneling junctions (FTJs) and ferroelectric field effect transistors (FeFETs) have increased variability from the nonuniformity of the polycrystalline ferroelectric layer and stochastic switching kinetics.[35] Engineering of materials, processing, and operation protocols could improve the variability of these devices.[36–38] The variability can also be partially compensated by SNN design such as the homeostasis mechanism[39] using more complex synapses and neurons. However, the variations of the modulation characteristics such as the threshold voltage could become a key challenge for achieving good reliability and high performance with spiking neural networks.[19] It is highly desirable to implement reliable time-dependent learning rules with low variability, low energy consumption, fast operation speed, and lean footprint.

Electrochemical ionic synapses (EIS), also known as electrochemical random-access memory (ECRAM), are three-terminal programmable resistors with conductance controlled deterministically by electrochemical charge insertion.[40–47] The conductance of a channel material is modulated by ion and electron insertion/extraction, controlled by an applied electrochemical potential difference at a gate terminal with respect to the channel.[47] Due to their low energy consumption, low variability, and deterministic charge-controlled conductivity modulation, EIS devices are being studied and pursued for their potential to enable energy-efficient analog neural networks.[40,41,43] Using the intrinsic nonlinearity of EIS devices could be one effective way to emulate STDP in an energy-efficient and controllable manner. To date, achieving STDP with EIS has not been shown in the field, and demonstrating this is the goal of this paper. EIS devices have a very strong nonlinear response to applied voltage.[45,42] This arises from the nonlinear electric field dependence of ion transport and interfacial charge transfer kinetics in EIS, as well as the nonlinear dependence of electronic conductivity on the concentration of ions and electrons inserted in certain channel materials.[44,47] This nonlinear kinetics of EIS presents an opportunity to achieve timing-dependent weight updates in a synaptic device as needed for STDP and SNNs.

In this paper, we leverage the nonlinearity of EIS to achieve various forms of STDP learning rules. We use proton as the working ion in the EIS devices.[44,45,48] We reliably predict and design the form of the STDP function based on the pre-and post-neuron signals superimposed at the gate of EIS. We show that the timing-dependent weight update allows heterogeneous choices of STDP function shapes in synapses from a single neuron connecting to different post-synaptic neurons. We control the response timescales from milliseconds down to nanoseconds, with lower variability and lower energy consumption than other STDP attempts in the field. Our approach here leverages the intrinsic nonlinearities of the EIS device, without the need for transistors at each synapse, so the system has reduced footprint and fabrication complexity. These results point to the potential of EIS to serve as programmable synapses to enable reliable hardware implementations of SNN with high energy efficiency and high throughput.

2. Results and Discussion

2.1. Strongly Nonlinear Response of Electrochemical Ionic Synapses

In this study, we focus on EIS devices using protons as the working ion.[44,45,48] **Figure 1a–c** shows the device structure and microscope images of an example EIS device fabricated in this work (see Experimental Section for device fabrication process). The devices consist of a 10 nm thick WO_3 channel, a 7–14 nm thick yttria-stabilized zirconia (YSZ) layer as the solid-state electrolyte, and a 15 nm thick top Pd layer as the hydrogen reservoir layer and the gate. Source and drain contacts are made of Au with a Cr adhesion layer, connecting to the side of the channel. The channel lateral dimensions varied between 3 and 40 µm for the width and length in different EIS devices used. The WO_3 channel has tunable electronic conductance that is determined by the proton concentration in it, as we have shown in our earlier work.[44] The YSZ electrolyte is fully oxidized, as seen from the Zr 3d and Y 3d X-ray photoelectron emission peaks (Figure 1d,e), showing that the Zr and Y have valences of +4 and +3, respectively. The YSZ electrolyte is largely amorphous, as seen from the X-ray diffraction pattern in Figure 1f, and this is consistent with a film deposited at room temperature. The fully oxidized YSZ electrolyte is insulating for electrons, but its amorphous and likely nanoporous nature makes it conductive to protons through absorbed —OH groups.[49] The Pd layer becomes a hydrogen reservoir in the form of PdH_x when exposed to hydrogen-containing forming-gas prior to experiments.[44]

The application of a gate voltage that is higher than the open circuit voltage (−0.3–0 V, depending on the proton concentration in the WO_3 channel[44]) oxidizes hydrogen in PdH_x and drives the protons from the reservoir through the electrolyte into the channel layer with electrons flowing through the external circuit from the gate to the channel. The electrons inserted into the WO_3 along with the protons, lead to the filling of in-gap states of WO_3 and increase its electronic conductivity.[44] The application of a gate voltage lower than the open circuit voltage reverses the process. Because of the small size of the proton and the high sensitivity of the WO_3 electronic conductivity to hydrogen concentration,[44] the device allows for high-speed (ns regime) modulation and high energy efficiency.[45] We have experimentally shown that these devices could be programmed reliably with very low energy consumption, close to 20 aJ per programming pulse for the proton

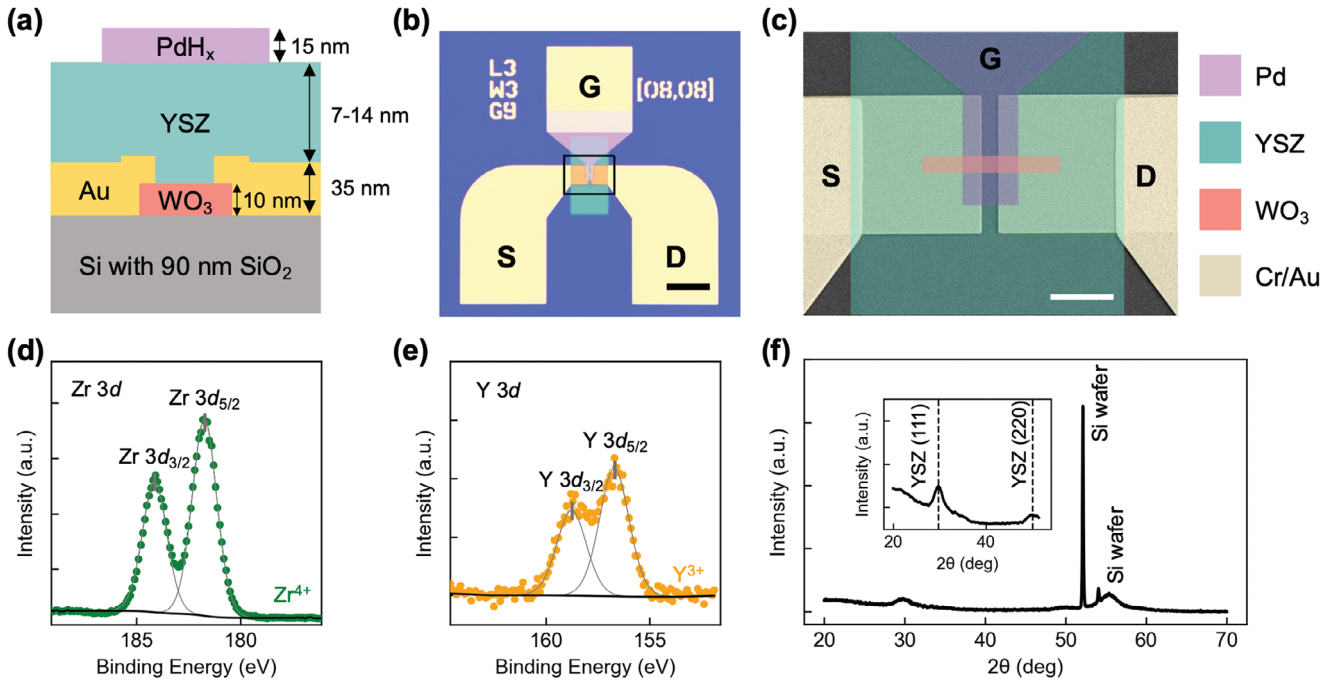

Figure 1. Structure and chemical characterizations of electrochemical ionic synapses (EIS) studied for emulating STDP functions. a) Schematic device structure with the gate (PdH_x), electrolyte (yttria-stabilized zirconia, YSZ), channel (WO_3), and source-drain (Au) contacts shown, and b) optical microscope image from the top of EIS devices experimentally characterized. S: source, D: drain, G: gate. The channel width and length are both 3 µm and the gate width is 9 µm. Scalebar, 50 µm. c) Top-view false-colored scanning electron microscope image of the device. Scalebar, 10 µm. d,e) X-ray photoelectron spectroscopy of the YSZ electrolyte centered at Zr 3d (d) and Y 3d (e). f). Grazing incidence X-ray diffraction pattern of the YSZ electrolyte layer. Inset, zoomed-in diffraction pattern near YSZ-related features. The diffraction pattern shows that YSZ is largely amorphous.

transfer during the peak voltage of the pulses, with order of fJ per pulse including the charging and discharging transients.[45] We use these protonic EIS devices to experimentally quantify the nonlinearity of the conductance change and leverage that nonlinearity to achieve timing-based conductance updates emulating different STDP forms.

The conductance change in an EIS has a strongly nonlinear dependence on the gate voltage when the gate voltage is away from the open circuit potential. This nonlinear dependence is a result of nonlinear ion transport through the electrolyte, nonlinear reaction kinetics at the interfaces as well as nonlinear dependence of the conductance of the channel on the inserted ion concentration.[44,47] When a strong electric field is present across the electrolyte, the energy barrier for ion conduction is lowered,[50] giving rise to a field-enhanced ionic conductivity, σ. The dependence of σ on the electric field, E through the electrolyte is approximately proportional to $\sinh(\frac{ql_xE}{2k_BT})$, where q is the ion charge, l_x is the hopping distance, k_B is the Boltzmann constant, and T is temperature. Similarly, the reaction kinetics at the interfaces can be described by the Butler–Volmer equation,[51] $j = j_0(e^{\frac{\alpha zFV_i}{RT}} - e^{\frac{-(1-\alpha)zFV_i}{RT}})$, where j is the reaction current density, j_0 is the exchange current density, α is the charge transfer coefficient for the interface, F is the Faraday constant, R is the ideal gas constant, z is the ion charge number, and V_i is the overpotential at the interface. When α is 0.5, the expression of j simplifies also to a sinh dependence on the local voltage such that $j \propto \sinh \frac{zFV_i}{2RT}$. This nonlinear voltage dependence has been experimentally observed for EIS devices with various ions.[45,42] The sinh relation has been used to explain and model the voltage dependence of conductance modulation for our EIS devices earlier.[45,47]

Figure 2a,b shows the conductance change of a device with a YSZ thickness (t_{YSZ}) of 14 nm, as a function of pulse duration (t_{pulse}) and pulse voltage (V_{pulse}). For the same V_{pulse}, the change in conductance achieved in each pulse, ΔG, scales nearly linearly with t_{pulse}, with small deviations. However, ΔG gets exponentially larger for higher V_{pulse}. For example, an increase of V_{pulse} from 2 to 4 V speeds up (requires a lower value of t_{pulse}) conductance modulation by ≈60 times, and an increase from 2 to 6 V speeds up by ≈1000 times. Figure 2c shows the rate of conductance change ($\Delta\dot{G}$) as a function of pulse voltage. In addition, temperature can introduce additional non-linearities and impact multiple aspects of device operation (see Section SI, Supporting Information for a discussion on the effect of temperature). Such nonlinear dependence of $\Delta\dot{G}$ on V_G enables the timing-based update of conductance at the EIS, as we describe and illustrate below.

2.2. Timing-Dependent Programming of Nonlinear EIS Devices

To implement timing-dependent learning rules with EIS, we apply the linear superposition of the voltage waveforms from the pre-and post-synaptic neurons to the gate of the EIS. The time dependence of the pre-and post-synaptic neuron firing waveforms is designed to target different forms of STDP. **Figure 3**a shows a simple and energy-efficient way to implement the linear

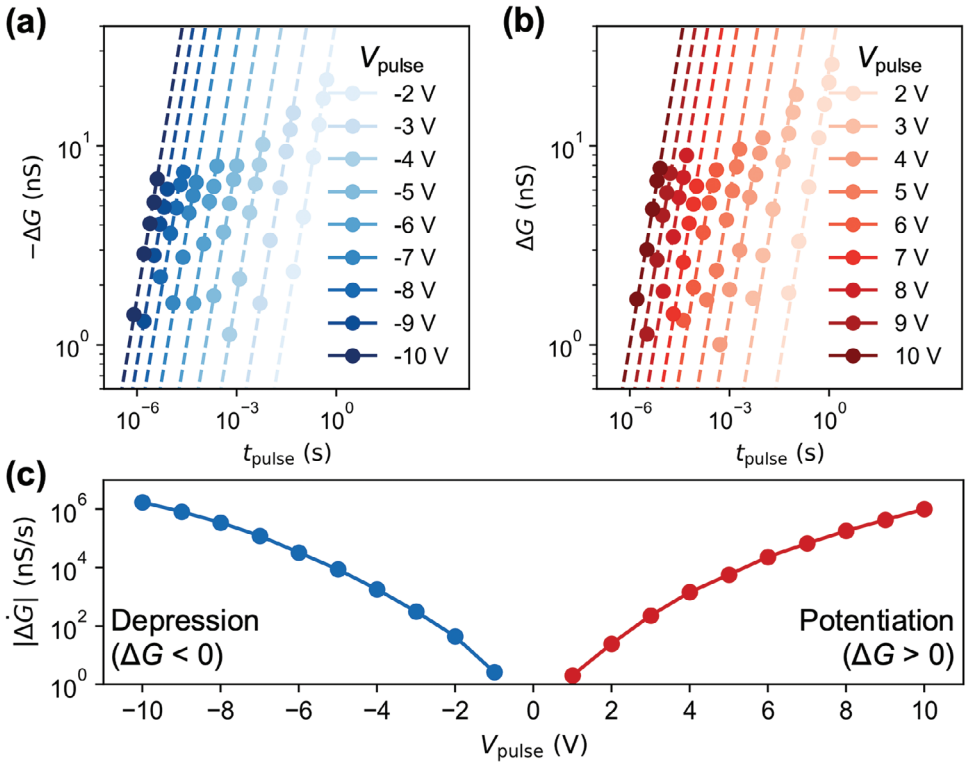

Figure 2. Strong nonlinear response of EIS to the applied gate voltage. a,b) Channel conductance change (ΔG) as a function of pulse duration (t_{pulse}) and pulse voltage (V_{pulse}). Dashed lines are linear fits of the log-log plot of ΔG versus t_{pulse}. (a) For V_{pulse}<0. (b) For V_{pulse}>0. c) The rate of conductance change $\Delta \dot{G}$ as a function of V_{pulse}, obtained from the intersect of the linear fit on the log-log plot in (a) and (b).

superposition. A voltage divider is formed across the voltage waveforms from the pre-synaptic neuron (V_{pre}) and the post-synaptic neuron (V_{post}). For the voltage divider to produce the desired linear superposition of the voltages, the resistance of the resistors, R, needs to be much smaller than the gate resistance of the EIS device. The requirement is trivial to satisfy because the gate resistance of EIS devices is usually very high, for example, more than 10 GΩ for a submicron device in ref. [45], because the electrolyte is electronically insulating (see Section SII, Supporting Information for achievable time scales). The resulting V_G waveform depends on the relative timing (Δt) of the firing of the pre-and the post-synaptic neurons. Here we define $\Delta t = t_{post} - t_{pre}$, where t_{post} and t_{pre} are the times when the post- and pre-synaptic neuron fire, respectively. Δt is positive when the post-neuron fires after the pre-neuron. With an R-value sufficiently small, the gate voltage can be approximated by the formula $V_G = (V_{pre} + V_{post})/2$. The voltage divider structure does not consume energy when the neurons are in the resting state, and energy is only consumed during spiking events. (See Section SIII, Supporting Information for alternative circuit approaches).

Figure 3b–d shows an example of timing-based conductance modulation of a single EIS synapse to implement an STDP learning rule. Here we implement a common STDP form, where the conductance of a synapse increases for $\Delta t > 0$ and decreases for $\Delta t < 0$. To achieve this form of STDP (Figure 3d), the V_{pre} and V_{post} waveform can be set to as shown in Figure 3b. The V_{pre} and V_{post} waveforms are designed such that they do not induce a large conductance change of the synapse if they fire alone. The self-compensating characteristic of V_{pre} and V_{post} waveforms ensures there is a significant net conductance change only when these two signals fire close enough and overlap in time. The shape of the V_{pre} and V_{post} are designed to enable targeted STDP forms, and the approach for designing such waveforms is described later in the section on obtaining different STDP forms. Depending on the timing of the firing of the pre-and post-synaptic neurons, the gate voltage ($V_G(t) = (V_{pre}(t) + V_{post}(t))/2$) takes different waveforms for different Δt values, as shown in Figure 3c. In the experiments, the superimposed waveforms were calculated and applied to the gate of the EIS device using a function generator. After the $V_G(t)$ waveform is complete, 0 V was applied to the EIS device as the resting potential, rather than an open circuit, for practical operation. Most of the conductance change takes place right after the spiking event, although the ΔG quantified here is the conductance difference between right before and 20 s after the pre-synaptic neuron signal fires. (The delay time to read does not reflect the timescale of the conductance modulation). The resulting ΔG as a function of relative timing, Δt is shown in Figure 3d. The amplitude of modulation is highest when the pre-and post-synaptic neurons fire close to each other (the absolute value of Δt is small). The resulting behavior clearly emulates the canonical STDP behavior seen in biological neural circuits. The ΔG in Figure 3 is intentionally kept small to be comparable to the STDP in synapses of the brain, where a single spiking event introduces only a small synaptic strength change.[17] The modulation ratio can be tuned by starting from different conductance levels, using waveforms with varying voltage or duration, and by continuously

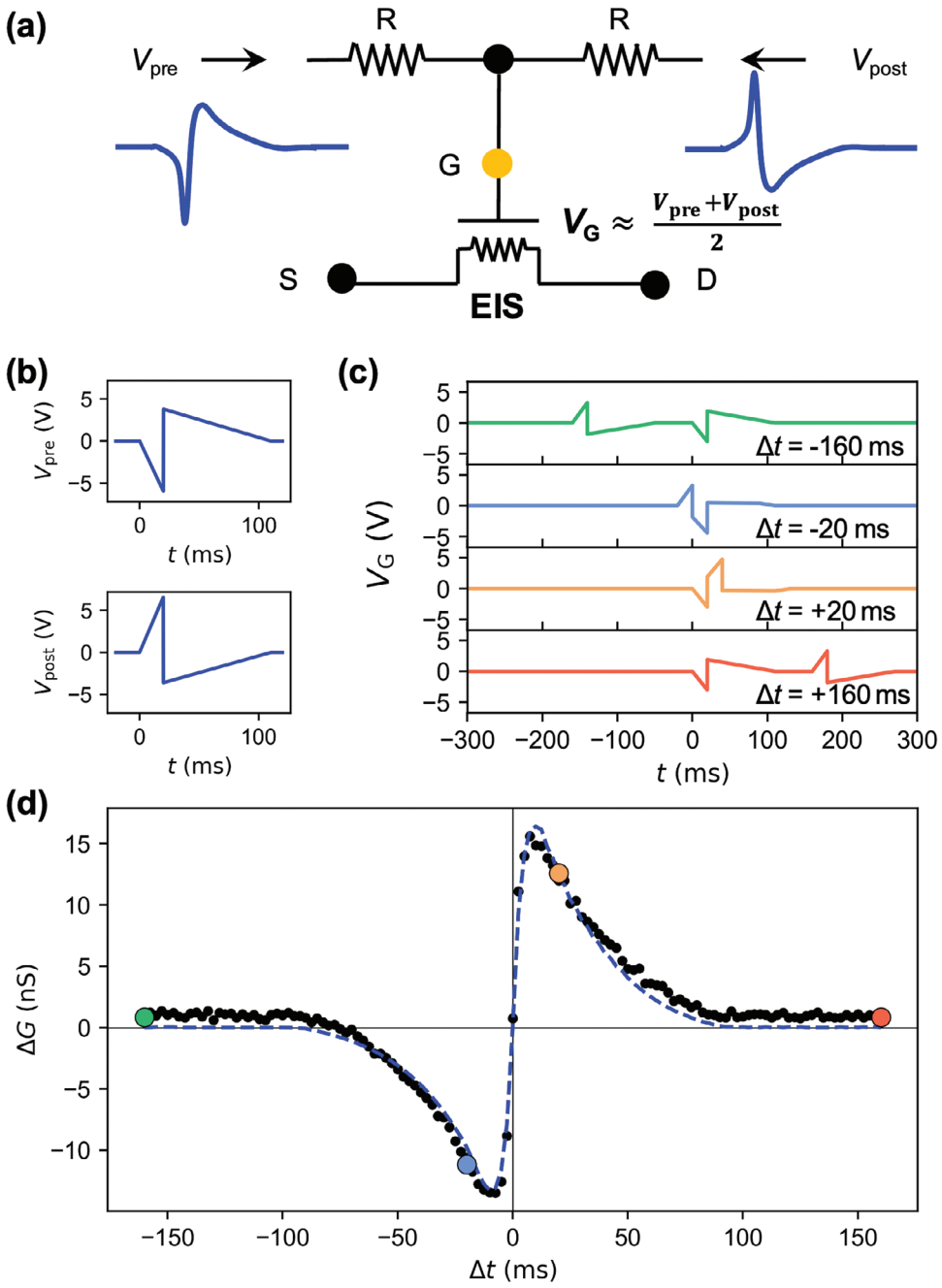

Figure 3. Timing-dependent programming of the EIS devices. a) The circuit used here to implement a linear superposition of voltage signals from the pre- and post-synaptic neurons. b) Waveforms of $V_{pre}(t)$ and $V_{post}(t)$ to achieve the canonical STDP function shown in (d). c) The waveforms at the gate terminal (V_G) for $\Delta t = -160$ ms, -20 ms, $+20$ ms, and $+160$ ms (top to bottom). d) Conductance change (ΔG) after the firing of both the pre- and post-synaptic neurons, as a function of the relative timing of firing, $\Delta t = t_{post} - t_{pre}$, where t_{post} and t_{pre} are the times when the post-and pre-synaptic neuron fire, respectively. The black points are experimental data, and the dashed line is the modeled and calculated ΔG. The ΔG was calculated as the integration of the conductance change rate at each time segment multiplied by a scaling factor of 0.7 (see text for modeling of ΔG). The colored points correspond to the conductance change from the Δt and the V_G waveforms at four different Δt values shown in (c).

spiking to cause cumulative and larger changes in conductance as discussed in a later section. In addition, we maintain the channel conductance in the ≈nS range, as this is the desirable and practical conductance level outlined in ref. [52]. This range prevents excessive current in metal lines and achieves low energy consumption in crossbar arrays. The devices offer flexibility in conductance, tunable over more than seven orders of magnitude by adjusting the ion concentration.[44] Additionally, the conductance can be adjusted by modifying the channel's aspect ratio (see Section SIV, Supporting Information).

The shape of the timing-dependent conductance change curve can be qualitatively explained by the nonlinear dependence of

the channel conductance change on the gate voltage. Because the conductance change is much greater at higher voltage, as explained above from the nonlinearity of the EIS, the conductance change from the portion of the $V_G(t)$ waveform with a high voltage amplitude dominates. When Δt is close to 0 (e.g., $\Delta t = 20$ ms, and $\Delta t = -20$ ms in Figure 3c), the conductance change is dominated by the large positive or negative voltage peak. When Δt is farther away from 0, the peak voltage becomes smaller, and the net conductance change becomes much smaller.

We model the time-dependent response of the EIS, to predict the learning curve from different $V_G(t)$ waveforms, and to design $V_{pre}(t)$ and $V_{post}(t)$ Waveforms. The STDP function can be calculated using the nonlinear dependence of conductance change on the gate voltage of EIS devices. If the spiking events of the pre- and the post-synaptic neuron take place at the same time, at $t = 0$, the waveforms are denoted as $V^0_{pre}(t)$ and $V^0_{post}(t)$ (such as those shown in Figure 3b). If the post-neuron spikes with a delay Δt relative to the pre-neuron, then we have $V_{post}(t) = V^0_{post}(t - \Delta t)$ and $V_{pre}(t) = V^0_{pre}(t)$. The gate voltage waveform is therefore $V_G(t) = \frac{V_{pre}+V_{post}}{2} = \frac{V^0_{pre}(t)+V^0_{post}(t-\Delta t)}{2}$. Assuming there is no interaction between the time segments, we can calculate the change of conductance of the EIS as an integral of the rate of conductance change for each time segment:

$$\Delta G = \int \Delta \dot{G}\left(V_G(t)\right) dt = \int \Delta \dot{G}\left(\frac{V^0_{pre}(t) + V^0_{post}(t-\Delta t)}{2}\right) dt \quad (1)$$

where $\Delta \dot{G}(V_G)$ is the rate of conductance change that depends on the gate voltage, V_G, and the limit of integration covers the whole period of the two spiking events. The rate of conductance change $\Delta \dot{G}(V_G)$ is interpolated from the experimentally measured data in Figure 2c. The calculated time-dependence of the STDP curves (dashed lines in Figure 3d) show good agreement with the experimentally measured STDP from the EIS devices. We note that, after the conductance change from all Δt values is calculated through the integration in Equation (1), they are multiplied by a common factor between 0.5 and 0.7, such that the modeled conductance peak amplitude matches the experimental data. For a given combination of $V^0_{pre}(t)$ and $V^0_{post}(t)$, a constant scaling factor is used. We attribute the discrepancy between the numerically modeled and experimentally measured STDP amplitudes to the complex dynamics of EIS. The conductance change of EIS cannot be treated as a simple integration over each time segment assumed to be non-interacting, also seen in Figure 2a,b. The behavior could be due to the intrinsic dynamics of the devices, including the capacitive processes such as the accumulation of ions at the interfaces.[47]

2.3. Implementing Different Bio-Realistic STDP Forms

The diversity and versatility of biologically observed STDP forms demand high flexibility on the part of the hardware. We experimentally demonstrate four typical STDP shapes by changing the waveforms of V_{pre} and V_{post}. A sketch of STDP forms that are observed in the brain, the experimentally measured STDP curves from our EIS circuit, and the V_{pre} and V_{post} waveforms used for each SDTP form, are shown in **Figure 4**. The demonstrated STDP forms include: the conventional antisymmetric STDP form characterized in hippocampal cultures[17] (Figure 4a), long-term potentiation-only STDP form found at CA3–CA1 hippocampal synapses[53] (Figure 4b), bidirectional symmetric STDP form found in GABAergic hippocampal synapses[54] (Figure 4c) and antisymmetric STDP form with a region of no plasticity in a temporal range near $\Delta t = 0$, observed in inhibitory synapses in the entorhinal cortex[55] (Figure 4d). The dashed lines in Figure 4a–d show the simulated STDP (using the approach described above), which is in good agreement with the experimentally measured STDP data. The good agreement between the modeled and experimental results suggests that the timing-dependent conductance update is reliable and predictable. In biological neurons, the electrical signals that correspond to spiking events generally take similar forms[56] although they can produce different STDP functions. This is in contrast to the very different V_{pre} and V_{post} waveforms used here to capture different STDP forms. The origin of biological synapses showing different STDP functions from similar electrical signals has been attributed to chemical signals such as calcium concentration transients.[57] We cannot capture the details of chemistry at each synapse since the EIS device materials and ions used are the same for each STDP form. Instead, we consider the V_{pre} and V_{post} used here to represent a convolution of the spiking electrical signal and the local chemistry and molecular pathways that the STDP originates from.[58]

2.4. Heterogeneous Learning Rules and Dopamine-Modulated STDP

In biological systems, different STDP forms take place at synapses connecting the same pre-synaptic neurons to different post-synaptic neuron types.[22,23] In addition, the STDP form can be altered by neuromodulators including dopamine and acetylcholine.[59,60] We show that EIS is conducive to emulating these complex behaviors. We first emulate heterogeneous STDP rules using our EIS circuit (**Figure 5**a,b). The V_{pre} from the pre-synaptic neuron (labeled "Pre neuron") is shared by two synapses (Synapse A and B), but these synapses receive different V_{post} waveforms from different post-synaptic neurons (labeled "Post neuron A" and "Post neuron B"). Therefore, the linear superposition of the V_{pre} and V_{post} is different in symmetry and shape on the EIS representing Synapse A and Synapse B. As a result, we obtain different STDP forms for the two synapses, shown in Figure 5b. This result closely resembles, for example, the STDP variations observed in synapses at parallel fiber inputs onto fusiform and cartwheel cells.[22]

EIS can also be used in the emulation of dopamine-modulated STDP behavior. A potential local circuit approach is exemplified in Figure 5c,d, where the pre- and post-synaptic neuron signals are multiplied by factors α_{pre} and α_{post}, respectively. These factors emulate the dopamine level of each neuron. Figure 5d shows the simulated STDP forms when α_{post} is modulated from +1 to −1 while keeping α_{pre} constant as 1. The input V_{pre} and V_{post} waveforms from Figure 3b are used for the simulation. The results show that the STDP shape changes from the conventional asymmetric with $\alpha_{post} = 1$ on the right, to become symmetrical and negative near $\Delta t = 0$ with $\alpha_{post} = -1$ on the left. A second approach is to use a third signal related to the dopamine level that

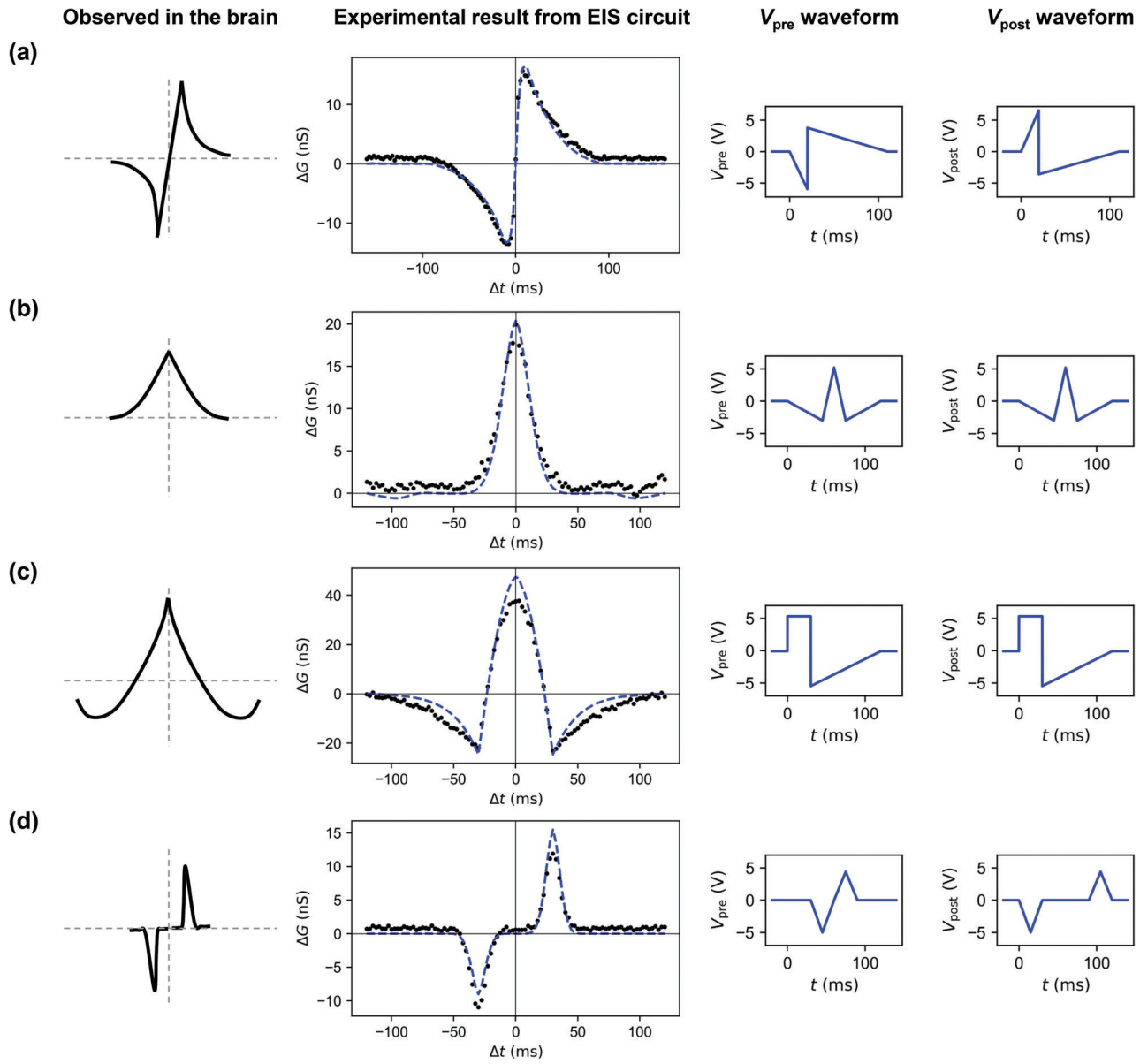

Figure 4. Emulating different STDP forms observed in the brain by varying the V_{pre} and V_{post} waveforms. a) The conventional antisymmetric STDP form is characterized in hippocampal cultures.[17] b) Long-term potentiation only STDP form found at CA3–CA1 hippocampal synapses.[53] c) Bidirectional symmetric STDP form, found in GABAergic hippocampal synapses.[54] d) Antisymmetric STDP form with a region of no plasticity in a temporal range near $\Delta t = 0$, observed in inhibitory synapses in the entorhinal cortex.[55] For each type, from left to right: the sketch of the targeted STDP shape, the STDP learning curve obtained from experimental (black points) and simulated data (dashed lines), and the V_{pre} and V_{post} waveforms to obtain the targeted STDP form.

can be superimposed onto the V_{pre} and V_{post} of each synapse. Simulated examples of dopamine-modulated STDP similar to those in biological observations, are shown in Figures S2 and S3 (Supporting Information).

2.5. Cumulative Modulation and Consistent Cycling from STDP

Long-term potentiation (LTP) involves a persistent strengthening of synapses depending on recent patterns of activity, while long-term depression (LTD) involves a persistent weakening of the synapse strengths. These mechanisms are key to synaptic plasticity, which is fundamental to learning and memory. To illustrate the cumulative effect of multiple spiking events, it is essential to examine continuous spiking in the context of LTP and LTD. **Figure 6** shows the results of EIS conductance modulation from continuous spiking, where the time delay, Δt, controls the direction of the conductance update, and the process was repeated for multiple cycles. Positive Δt spiking events result in a cumulative increase in conductance, while negative Δt events result in a cumulative decrease. The results clearly demonstrate the cumulative effect of multiple spiking events. Furthermore, the

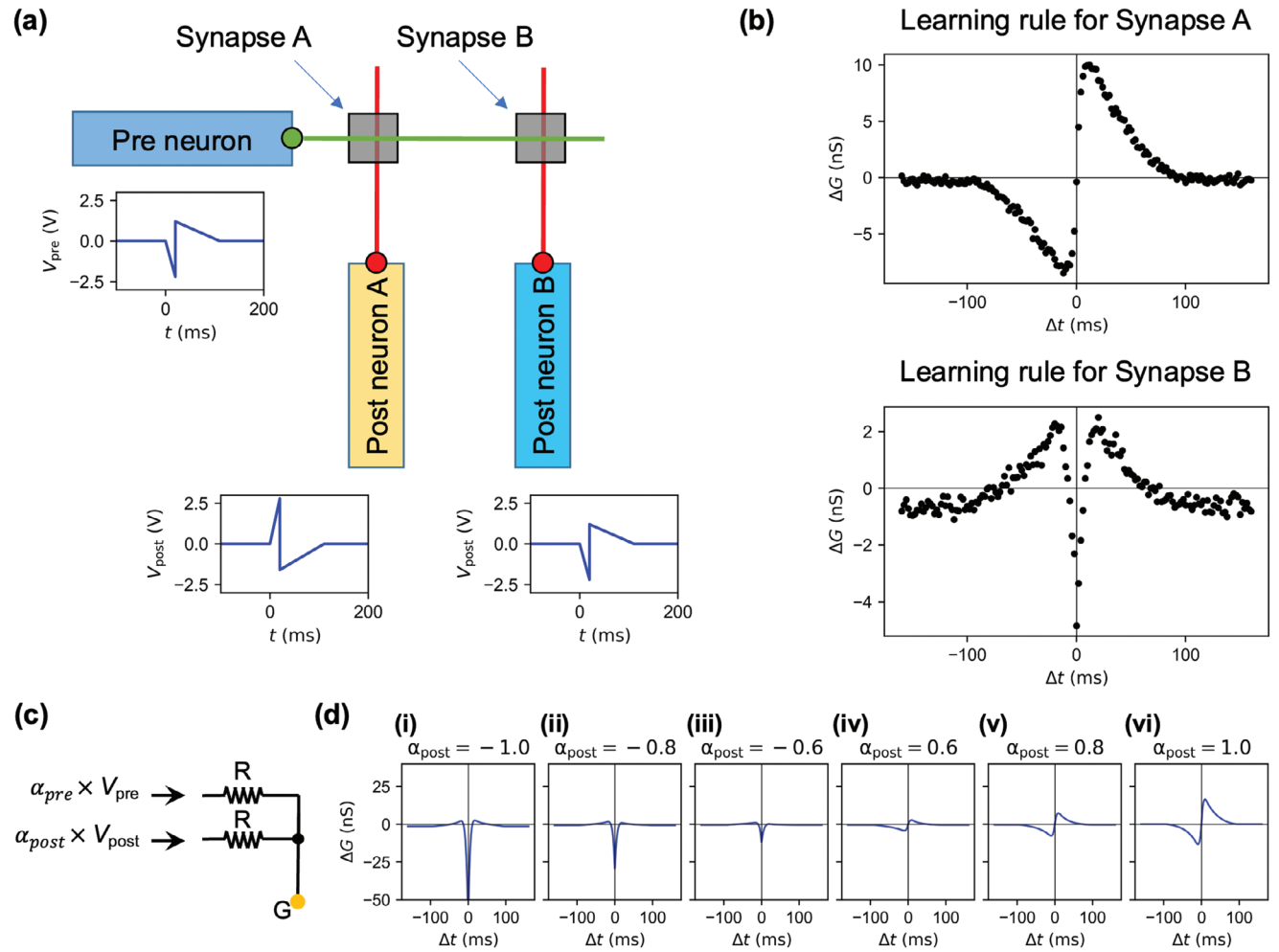

Figure 5. Heterogeneous and evolving STDP. a) Schematic configuration to implement heterogeneous STDP. Different STDP forms are obtained at two EIS synapses (Synapse A and B) connecting the same pre-synaptic neuron (Pre neuron) to two different post-synaptic neurons (Post neuron A, and Post neuron B). The voltage waveforms for the V_{pre} and V_{post} of the corresponding neurons are shown. b) The resulting STDP forms at the two synapses, A and B. c) Circuit for emulating dopamine-modulated STDP scales the pre- and post-synaptic neuron signals that are combined to serve as V_G of the EIS. d) Simulated STDP forms as a function of the scaling factor of the post-synaptic neuron (α_{post}). α_{post} changes from −1 (i) to +1 (vi), while the scaling factor for the pre-synaptic neuron (α_{pre}) is kept at 1.

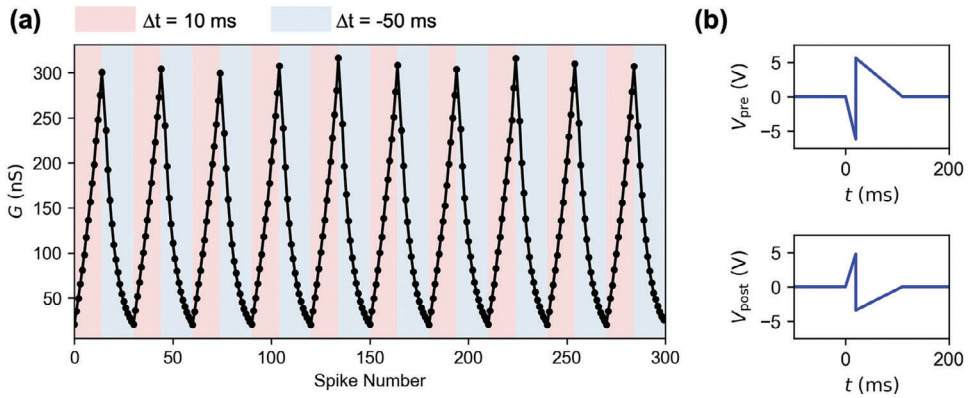

Figure 6. Cumulative LTP and LTD from continuous spiking events. a) Conductance changes for continuous spiking events with varying Δt. The conductance increases with positive Δt (LTP) and decreases with negative Δt (LTD), showing the cumulative and consistent modulation. The conductance is cycled between low and high states through alternating LTP and LTD events over 10 cycles. b) Waveforms of $V_{pre}(t)$ and $V_{post}(t)$ to generate LTP and LTD in (a).

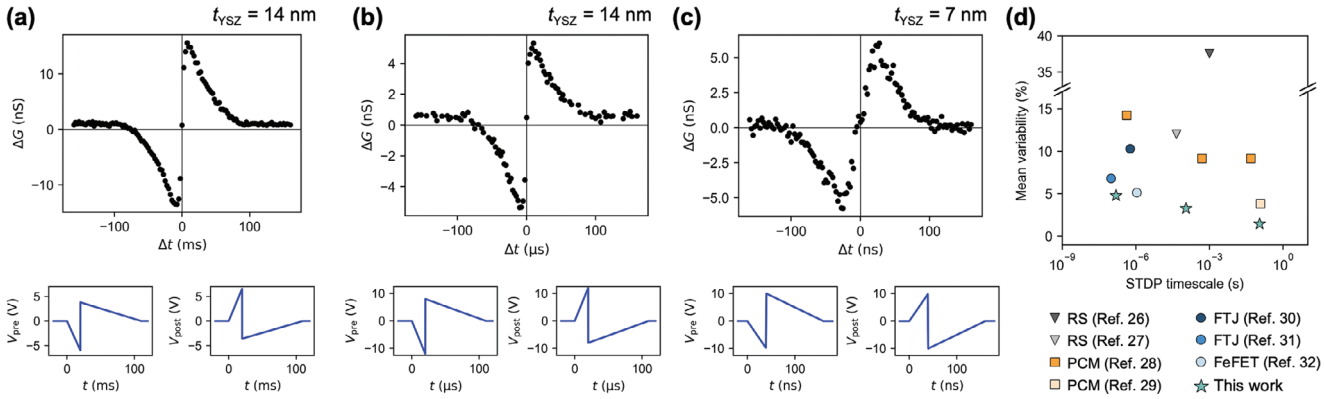

Figure 7. Experimentally measured STDP with timescales from milliseconds down to nanoseconds. For each time scale, the ΔG versus Δt (top) and the waveforms for V_{pre}(t) and V_{post}(t) (bottom) are shown. a). Time scale regime of 100 ms, with a peak voltage level of 6.5 V using a device with a YSZ electrolyte thickness (t_{YSZ}) of 14 nm. b) Time scale regime of 100 μs, with a peak voltage level of 10 V using a device with t_{YSZ} = 14 nm. c) Time scale regime of 100 ns, with a peak voltage level of 10 V using a device with t_{YSZ} = 7 nm. d) Comparison of variability and programming timescale for synaptic devices implementing STDP, including the EIS devices in this work, and devices based on resistive switching (RS),[26,27] phase-change materials (PCM),[28,29] ferroelectric tunnel junctions (FTJ),[30,31] and ferroelectric field effect transistors (FeFET).[32]

conductance can be cycled between low and high states by alternately applying positive (LTP) and negative (LTD) spiking events, with a max/min ratio greater than 10x and excellent consistency. The conductance max/min ratio can be further tuned by using pulses of larger voltage or longer durations, as shown in Figure 2. The versatility and consistency in the cumulative changes indicate that our EIS devices can effectively emulate the long-term plasticity observed in biological synapses, providing a robust foundation for implementing more complex learning rules and functionalities in SNN hardware.

2.6. Energy Efficient STDP with Low Variability and Flexible Timescales from Milliseconds to Nanoseconds

The energy consumption, variability and speed of STDP using our EIS circuit are important performance characteristics for implementing SNN hardware. We harness the fast operation speed of EIS devices (down to nanoseconds), low energy consumption and the intrinsic low variability and deterministic nature of the conductance modulation, and demonstrate that the EIS devices can achieve a good combination of the three.

Due to the strong field enhancement of the transport and interfacial reaction kinetics, the timescale of the conductance modulation can be tuned by the voltage amplitudes of the V_{pre} and V_{post} waveforms, by the thickness of the electrolyte, and by interface chemistry. As shown in **Figure** 7a–c, the canonical STDP behavior is implemented experimentally at a timescale ranging from milliseconds to nanoseconds. Millisecond timescales are more relevant for biological systems, and nanosecond timescales enable neuromorphic computing devices that potentially react and learn a million times faster than biological systems.

To assess the variability of the devices, we take the ΔG versus Δt data and calculate the mean absolute difference of the measured ΔG from the smooth curve fitted to the experimental STDP data. If the device has no variability, the resulting experimental ΔG versus Δt should follow a smooth curve, because the V_G waveform changes smoothly with Δt, and thus we should expect 0 (zero) difference between the measured ΔG and the smooth fitted curve. Any non-zero difference is a measure of the variability among each V_G applied to the device at each Δt. This is akin to the cycle-to-cycle variability of memristive devices.[61] This simple metric allows us to compare the variability of our devices to other non-volatile synaptic devices with published STDP results.[26–32] We characterize the timescales of the STDP by the length of voltage waveforms applied. A comparison of variability and STDP timescale, including values calculated based on the ΔG versus Δt data of our devices in Figure 7a–c and extracted from published results, is shown in Figure 7d. Importantly, we consistently achieve lower variability (<5%) at all timescales with the EIS, compared to other mechanisms (RS, PCM, FTJ, FeFET) reported to emulate STDP in the literature. Additionally, we evaluated the device-to-device variability for STDP implementation (see Section SVI, Supporting Information) and found a variability of ≈6%. This is a remarkably low variability, given that it is quantified at the very low conductance regime (10–100 nS), much lower than the variability of other device types, which never quantified variability at this low of a conductance target range, as we summarize in **Table 1** below, and it is well below the target maximum variability value for reliable training of networks.[52] We also believe that this variability of EIS devices can be brought down even more by leveraging the state-of-the-art fabrication technologies in the industry, which surpass those at university laboratories.

We estimate the energy consumption of the STDP-performing EIS devices. Since no power is needed at rest when there are no spiking events, the idling power consumption is zero for the synapses. The energy associated with electrochemical proton insertion is estimated to be below 1.0 fJ per spiking event, using data for WO_3 intercalation,[44] and by assuming that a peak voltage (10 V) is applied during the whole process. In addition, energy is consumed by the resistors, and the charging and discharging of the capacitance of the EIS gate need to be considered. We calculated the full energy consumption of the circuit by integrating the power during the spiking events (see Section SVII, Supporting Information). The calculation shows that the energy consumption of each spike event is ≈27–54 fJ for the STDP behavior

Table 1. Advantages of utilizing EIS to implement STDP. The comparisons are with respect to RRAM as the most commonly studied device concept, and to other best contender device concepts.

Characteristics	EIS [this work]	Best contender	RRAM
Device-to-device variability	≈6% (10 nS < G < 100 nS)	FeFET, 40% (G ≈ 2 µS)[66]	80% (G ≈ 10 µS)[67]
Programming speed	160 ns	FTJ, 100 ns[31]	1 µs[68]
Energy consumption per spiking event	< 60 f]	FTJ, ≈2 pJ[31]	≈7 pJ[62]

shown in Figure 7c. We estimated the energy consumption of STDP by other types of resistance switching devices from literature using waveforms and testing protocols extracted from the plots, the estimated energy consumption per spiking event are: ≈7 pJ, ≈150 pJ, ≈2 pJ, and ≈0.9 nJ for RRAM,[62] PCM,[29] FTJ[31] and FeFET,[32] respectively. The comparison shows the superior energy efficiency of EIS for implementing STDP.

Major advantages of utilizing EIS to emulate STDP are summarized in Table 1, in comparison to other device concepts that attempted to emulate STDP in the field. The comparison shows that EIS simultaneously provides the least variability and the least energy consumption while being able to operate at a speed regime of nanoseconds. Furthermore, for the protonic EIS focus of our paper, all the functional materials and fabrication processes are CMOS-compatible. The oxides in the devices are deposited with scalable sputtering processes at room temperature, and the Au layers used for electrical contacts can be replaced with CMOS-compatible materials such as W. Pd has been used in CMOS processes as a contact material.[63] Additionally, the Pd top gate can be replaced with a WO_3 layer to form a symmetric device,[64,46] eliminating the need for Pd metal. These silicon-compatible materials and processes facilitate integration with peripheral circuits, bringing the device closer toward commercial applications.

3. Conclusion

We leverage nonlinear ion dynamics and charge transfer reactions controllably in protonic EIS, to achieve spike timing-dependent weight programming. This allowed us to emulate different bio-realistic STDP functions at timescales tunable from milliseconds down to nanoseconds. The resulting STDP has very low energy consumption and lower variability than other hardware STDP implementations in the field. The EIS circuit also allows for heterogeneous STDP where the synapses from a single neuron can have different learning rules depending on the behavior of the post-synaptic neurons. The strongly nonlinear behavior of conductance modulation is general across EIS devices with different ions, so that a broad range of EIS ions, materials, and devices can be applied to emulate STDP. The approach could enable reliable SNN hardware implementations with high energy efficiency and high throughput.

4. Experimental Section

Device Fabrication: The EIS devices were fabricated on Si substrates with 90 nm thermal SiO_2 oxide. First, the channel was patterned using electron-beam lithography with polymethyl methacrylate (PMMA) resist. The WO_3 channel (10 nm thick) was grown by reactive sputtering using a W target in a gas environment with an $Ar:O_2$ ratio of 9.3:2.7 at 3 mTorr at room temperature, followed by liftoff. The source and drain contacts were patterned and deposited by electron-beam lithography and electron-beam evaporation of Cr 5 nm and Au 35 nm, followed by liftoff. The YSZ solid-state electrolyte (14 or 7 nm thick) was grown by RF sputtering from a YSZ (8 mol.% yttrium oxide doped zirconium oxide) target with $Ar:O_2$ ratio of 15:4 at 3 mTorr at room temperature, followed by photolithography and ion milling. Finally, the Pd reservoir layer was patterned and deposited with electron-beam lithography, and electron-beam evaporation followed by liftoff. The Pd layer becomes PdH_x when placed in the hydrogen-forming gas environment during testing.

Electrical Measurements: The samples were mounted, wire bonded to a custom-designed PCB, and placed in a gas-enclosed box with feed-throughs for making electrical connections to the devices. The box was filled with hydrogen-forming gas composed of 4% H_2 and N_2. The hydrogen content in PdH_x under the gas environment was estimated to be x≈0.65 at 20 °C.[65] The channel conductance was measured using a semiconductor analyzer (B1500A) with a bias voltage of 0.1 V, and the gate waveforms were generated by a SIGLENT 2000X function generator. Before each STDP measurement, the devices were first initialized to ≈1000 nS by applying voltage pulses to the gate, to have a consistent initial conductance state in the experiments.

Conductance Change Calculation from V_G Waveforms: The conductance change from a V_G waveform is calculated using Equation (1). The conductance change rate is interpolated from the experimentally measured data, such as that shown in Figure 2 in this work. To calculate the effect of a voltage waveform from a voltage, the waveform is first numerically sliced into segments of length τ, which is chosen so that τ is sufficiently small for each waveform. The conductance change from each time segment is then added up to get the final expected conductance change. After the conductance change from all Δt values is calculated, they are multiplied by a common factor: 0.7, 0.5, 0.65, and 0.7 for Figure 4a–d, respectively. The reason for this factor is explained in the manuscript.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrochemical ionic synapses, nanoionics, spike-timing-dependent plasticity, spiking neural networks

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