nature electronics

Article

https://doi.org/10.1038/s41928-025-01408-z

Residue-free wafer-scale direct imprinting of two-dimensional materials

Received: 6 September 2024

Accepted: 2 June 2025

Published online: 1 July 2025

Check for updates

Zhiwei Li[1], Xiao Liu[1], Jiayu Shi[2], Xiangbin Cai[1], Yan Zhang[1], Wenduo Chen[1], Yuhao Jin[1], Hao Jiang[1], So Yeon Kim[3], Chao Zhu[2], Ya Deng[2], Yanran Liu[4], X. Renshaw Wang[1,4], Taotao Li[5], Ju Li[3,6], Zheng Liu[2], Hongbing Cai[7] ✉ & Weibo Gao[1,4,8,9] ✉

Two-dimensional (2D) semiconductors have the potential to replace silicon in next-generation electronic devices. However, despite advances in proof-of-concept device demonstrations and wafer-scale crystal synthesis, the lack of a compatible residue-free patterning technology has hindered industrialization. Here we describe a metal-stamp imprinting method for patterning 2D films into high-quality wafer-scale arrays without introducing chemical or polymer residues. A metal stamp with a three-dimensional morphology is used to form a local contact at the stamp–2D interface. The process selectively exfoliates some of the 2D material while leaving 2D arrays on the growth substrate. Microscopy and spectroscopy characterizations confirmed the clean surface and undamaged crystal structure. A statistical analysis of 100 back-gated molybdenum disulfide (MoS_2) transistors and 500 top-gated logic circuits found a 20-times-lower variation of the threshold voltage compared to a reactive-ion-etching-based patterning process. The device yield on a 2-inch wafer was 97.6%.

Two-dimensional (2D) semiconductors are a promising material for continuing transistor scaling due to their atomic thickness and excellent electrical and optical properties[1–5]. The 2D materials community has achieved important advances in proof-of-concept demonstrations and the synthesis of wafer-scale crystalline films[6–12]. However, achieving high uniformity and yield in high-throughput electronic manufacture remains a key challenge in transitioning 2D electronics from laboratory-scale to industrial-scale integrated circuits[13,14]. Typically, chemicals and polymer residues introduced onto the 2D semiconductor surface during device manufacture act as sources of scattering or doping effects that disrupt the electrical properties of the 2D channels and, thus, reduce the uniformity and yield of large-area electronic devices.

Appropriate patterning techniques, during which a large-area thin film is divided into independent functional units, are a prerequisite for achieving complex logic functions and advanced integrated circuits. At present, patterning processes for 2D materials rely on traditional fabrication techniques, such as photolithography for masks and reactive-ion etching (RIE) for patterns. However, although these techniques are sufficiently robust for bulk materials, they are the dominant source of contamination on 2D surfaces in device manufacturing[15]. Specifically, chemical or polymer residues on the delicate surfaces of 2D materials reduce their electrical and optical performance[16–20]. Crosslinking caused by plasma acting on the polymer mask can further exacerbate this issue[21,22], creating challenges for realizing high uniformity, repeatability and yield of large-scale 2D electronics.

[1]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, Singapore. [2]School of Materials Science and Engineering, Nanyang Technological University, Singapore, Singapore. [3]Department of Nuclear Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA. [4]Division of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore, Singapore. [5]School of Integrated Circuits, Nanjing University, Suzhou, China. [6]Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA. [7]Hefei National Research Center for Physical Sciences at the Microscale, University of Science and Technology of China, Hefei, China. [8]Centre for Quantum Technologies, National University of Singapore, Singapore, Singapore. [9]National Centre for Advanced Integrated Photonics (NCAIP) Singapore, Nanyang Technological University, Singapore, Singapore. ✉e-mail: coldice@ustc.edu.cn; wbgao@ntu.edu.sg

https://doi.org/10.1038/s41928-025-01408-z

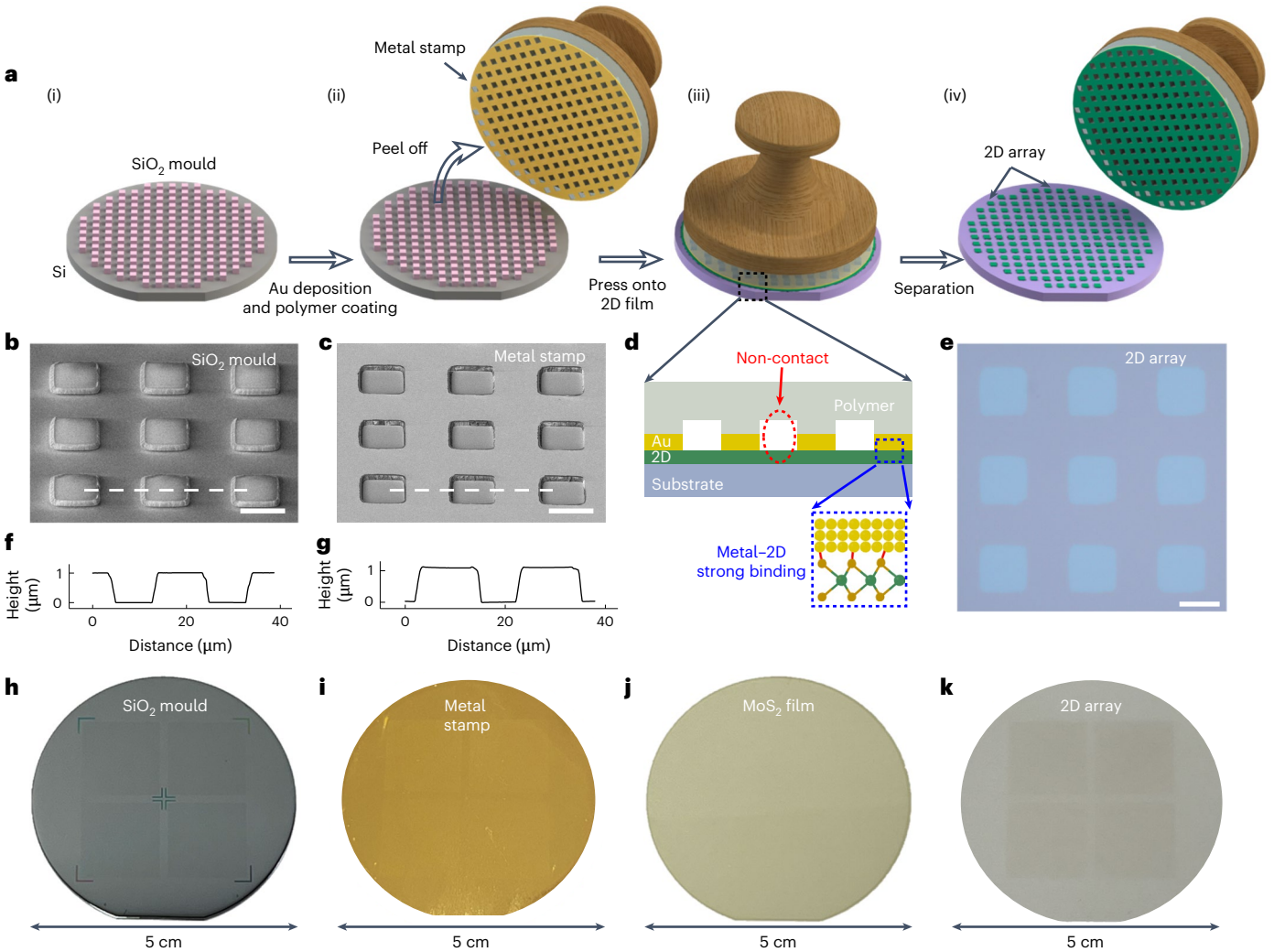

Fig. 1 | Schematic illustration of stamp-assisted imprinting of wafer-scale 2D materials. a, Method steps: (i) depositing the SiO_2 mould array onto a silicon wafer; (ii) depositing gold film onto the SiO_2 mould, spin-coating the surface with polymer to fabricate a 3D metal stamp and peeling off; (iii) pressing the 3D metal stamp onto a 2D wafer; (iv) separating the metal stamp from the 2D film to obtain 2D arrays. **b**,**c**, Scanning electron microscopy images of the SiO_2 mould (**b**) and metal stamp (**c**). The metal stamp inherits the inverted 3D morphology of the silicon mould. **d**, Schematic of a cross section of the 3D metal stamp pressed onto the 2D film and the local contact model. The metal–2D contact region forms a strong interaction, whereas the 2D material in the non-contact area retains its original state. **e**, Optical image of patterned monolayer MoS_2 arrays on a sapphire substrate. **f**,**g**, AFM measurements of the 3D morphology of the SiO_2 mould (**f**) and the metal stamp (**g**). **h**–**k**, Photographs of 2-inch stamp-assisted imprinting process: SiO_2 mould (**h**), metal stamp (**i**), MoS_2 film (**j**) and 2D array (**k**). Scale bars, 10 μm (**b**,**c**,**e**).

Considerable efforts have been invested in optimizing masks and upgrading patterning tools to reduce the residues of chemicals and polymers and, thus, minimize damage introduced by the patterning process. For example, a buffer layer has been introduced between the photoresist mask and the 2D channel to improve the efficiency of removing the mask[23]. However, this wet process does not completely eliminate chemical reagents and polymer residues to offer an intrinsically clean 2D surface. Alternatively, direct laser patterning[24] and scanning probe patterning[25–27] have been developed to directly etch 2D materials and, thus, avoid the use of a photoresist mask. Nevertheless, issues such as thermal accumulation in 2D materials caused by the focusing of a high-energy laser and the time consumed by wafer-scale patterning have hindered their application in large-scale integrated circuits.

In this article, we describe a metal-stamp imprinting method that was inspired by historic movable-type printing[28] and modern nanoimprint technology[29,30] for the residue-free patterning of wafer-scale 2D materials. First, a predesigned three-dimensional (3D) metal stamp was pressed onto a 2D film. The strong metal–2D interaction in the local contact region ensured exfoliation of the 2D material from the substrate, whereas in the non-contact region, the 2D arrays remained undamaged on the substrate. The patterning process does not use any photoresists or chemical reagents, thus enabling the wafer-scale, quick and high-quality patterning of 2D materials. We demonstrated our method on chemical vapour deposition (CVD)-grown molybdenum disulfide (MoS_2) and also show that it can be applied to CVD-grown tungsten diselenide (WSe_2) and tungsten disulfide (WS_2) films. The atomic cleanliness and crystallinity of the resulting 2D array surface was verified through photoluminescence (PL) spectroscopy, Raman spectroscopy, atomic force microscopy (AFM) and scanning transmission electron microscopy (STEM). We fabricated 100 back-gated MoS_2 field-effect transistors (FETs) for transport measurements. These devices exhibited improved electrical performance and uniformity compared to FETs made using a traditional RIE patterning method. Finally, we created wafer-scale logic circuits with a top-gated structure compatible with industrial fabrication processes. We realized a yield of 97.6% across 500 functional units.

https://doi.org/10.1038/s41928-025-01408-z

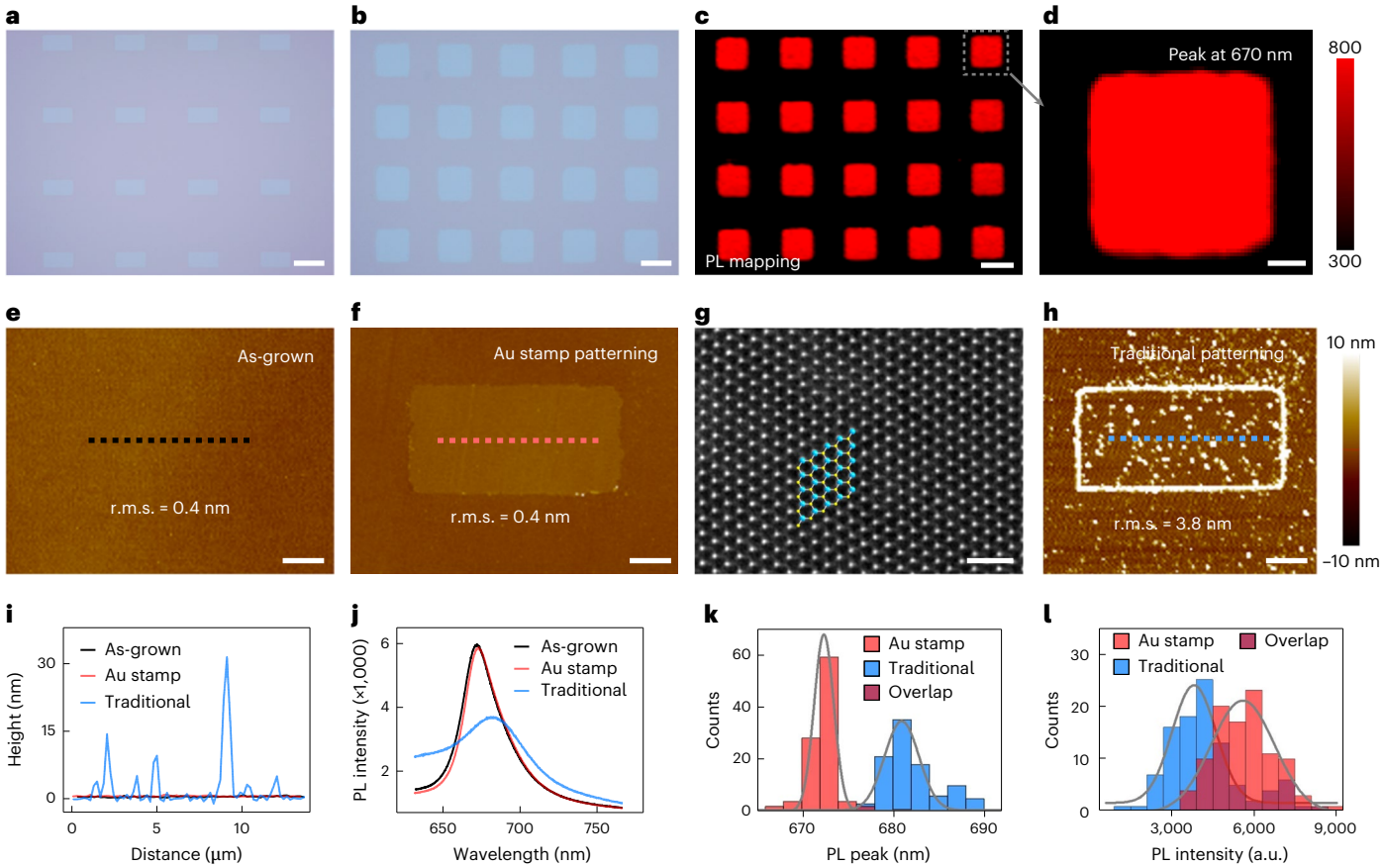

Fig. 2 | Characterization of MoS_2 array patterned through metal-stamp imprinting and traditional etching processes. a,**b**, Optical images of metal-stamp-patterned monolayer MoS_2 arrays with different shapes and spacing: rectangle (**a**) and square (**b**). **c**,**d**, PL intensity mappings of MoS_2 arrays, demonstrating uniform intensity across different arrays (**c**) and within one unit (**d**). **e**,**f**, AFM measurements of an as-grown MoS_2 film (**e**) and a stamp-patterned MoS_2 rectangle (**f**), both showing a clean surface with an r.m.s. roughness of 0.4 nm. **g**, Atomic-resolution HAADF-STEM image of stamp-patterned MoS_2. **h**, AFM measurement of traditional patterned MoS_2 with an r.m.s. roughness of 3.8 nm, which indicates that the patterning process may have left residues. **i**, AFM height profiles of as-grown and patterned MoS_2 (for the dotted lines in **e**, **f** and **h**). The stamp-assisted patterning method produced a flat profile like the as-grown film, whereas the traditional etching method produced a hilly profile due to residue. **j**–**l**, PL spectra and statistics distribution of monolayer MoS_2 obtained by different patterning methods. The stamp-patterned MoS_2 has a similar PL peak and intensity as the as-grown film, whereas traditional patterned MoS_2 shows a shifted peak and lower intensity (**j**). And the stamp-patterned samples demonstrate higher uniformity in PL peak (**k**) and PL intensity (**l**). Scale bars, 20 μm (**a**), 10 μm (**b**), 10 μm (**c**), 2 μm (**d**), 4 μm (**e**,**f**), 1 nm (**g**), 4 μm (**h**).

Residue-free direct imprinting of 2D film

Figure 1 shows the fabrication process of our residue-free direct imprinting method. First, a thick SiO_2 array (1 μm) was prefabricated on a polished silicon substrate as a 3D mould (Fig. 1a(i),b,h), using the standard photolithography and electron-beam deposition process (Methods and Supplementary Fig. 1). Subsequently, the metal stamp was fabricated by depositing a functional Au layer (50 nm) and spin-coating a supporting poly(bisphenol A carbonate) polymer layer onto the 3D SiO_2 mould surface layer by layer (Fig. 1a(ii)). The metal stamp was then mechanically peeled from the sacrificial Si substrate. The stamp inherited the inverted 3D morphology of the prefabricated mould (Fig. 1c,i), which was verified by AFM measurements (Fig. 1f,g). Next, the metal stamp was directly pressed onto the top of a CVD synthetic MoS_2 film (Fig. 1j). The 3D stamp formed a local contact model with the bottom 2D film (Fig. 1a(iii)). The contact regions had strong interface binding (between Au and MoS_2) due to the high adhesion energy at the Au–S interface (highlighted by the blue box in the inset of Fig. 1d), which was verified by our atomistic modelling (Supplementary Fig. 2) and previous reports[31–35]. The strong Au–2D binding force had enough strength to overcome the fracture shear stress of the 2D film and physically tore the local MoS_2 from the growth substrate. Note that this tearing process is like the 'tear-and-stack' technique often used for twist 2D heterojunctions[36,37]. We also conducted a similar boron nitride (BN) tearing test to confirm the weak fracture shear stress of the 2D lattice and support the proof-of-concept for metal tearing of 2D materials (Supplementary Fig. 3).

By contrast, the dented region of the 3D stamp did not make contact with the bottom 2D film (highlighted by the red ellipse in the inset of Fig. 1d), thus ensuring that the non-contacted 2D material retained its intrinsic state (Fig. 1d). On separating the metal stamp from the 2D film, the monolayer MoS_2 in the contact region was peeled away by the metal stamp, and the monolayer MoS_2 in the non-contact region remained on the substrate with its original quality, together creating a scalable monolayer MoS_2 array (Fig. 1a(iv),e,k and Supplementary Video). Compared to traditional methods, our metal-stamp imprinting method does not use a photoresist or solution process for the 2D film. Therefore, it maintains the intrinsic properties of the delicate 2D lattice. Our method avoids the quality or uniformity reduction that occurs when patterning 2D materials, and it is suitable for preparing large-scale and high-yield electronics. Note that the SiO_2 mould (Fig. 1a(i)) is reusable. After ten cycles of imprinting tests with the same mould, we still obtained a high-quality uniform 2D array, as shown in Supplementary Fig. 4.

https://doi.org/10.1038/s41928-025-01408-z

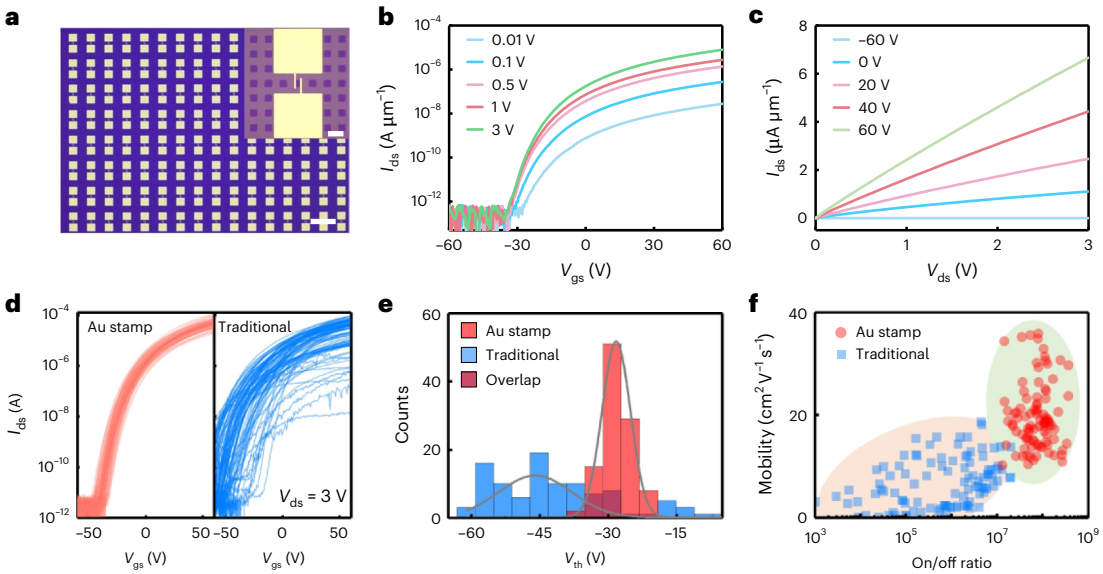

Fig. 3 | Electrical characterization of MoS_2 arrays. a, Optical image of back-gated MoS_2 transistor arrays. **b**,**c**, Transfer (**b**) and output (**c**) curves of a stamp-patterned monolayer MoS_2 device, demonstrating an on/off ratio of 10^8 and linear ohmic contact. **d**, Transfer characteristics of 100 stamp-patterned MoS_2 FETs and 100 traditional etching-patterned devices. **e**,**f**, Statistical distribution of V_{th} (**e**) and mobility versus on/off ratio (**f**). Scale bars, 200 μm (**a**), 20 μm (**a**, inset).

Characterization of MoS_2 array

By predesigning different 3D metal-stamps, we patterned various 2D arrays with different shapes or periods, including a rectangle, square, circle, ribbon, Hall bars and alphabetic characters (Fig. 2a,b and Supplementary Fig. 5). The monolayer nature of the stamp-patterned MoS_2 arrays was confirmed by the Raman frequency difference of 19.0 cm^{-1} between the E' peak (in-plane vibration) and the A' peak (out-of-plane vibration) and the AFM measurement (Supplementary Fig. 6). Furthermore, PL mappings of stamp-patterned MoS_2 arrays demonstrated their uniform intensity, indicating that the patterned MoS_2 was uniform, not only within each unit but also across arrays (Fig. 2c,d). In addition, due to the current rough edges of the SiO_2 mould and stamp, the edges of the patterned MoS_2 did exhibit a small inhomogeneity in the hundred-nanometre pattern process (Supplementary Fig. 7). However, based on our experience of commercial nano-imprinting technology and higher-precision lithography equipment, we expect to successively improve the 2D imprinting accuracy to the nanometre level.

The quality of the stamp-patterned monolayer arrays was comparable to an as-grown monolayer film and much better than achieved by the traditional RIE method, as evidenced by the AFM surface characterization and by the crystal quality characterized by STEM and PL spectra. As shown in Fig. 2e,f, the stamp-patterned MoS_2 flake had a pristine clean surface consistent with that of an as-grown MoS_2 film, with a root mean square (r.m.s.) roughness of 0.4 nm, indicating that our method had produced a residue-free surface. Furthermore, we performed an atomic-resolution high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) characterization of our stamp-patterned MoS_2, which found a lattice without damage or contamination (Fig. 2g and Supplementary Fig. 8). By contrast, the traditional RIE-patterned MoS_2 had random impurities on its 2D surface and substrate with an r.m.s. roughness of 3.8 nm (Fig. 2h,i), indicating that the photoresist and solution process of the traditional RIE patterning method leaves unavoidable residues.

Next, we performed PL spectrum measurements to further quantify the optical quality and uniformity of patterned samples from different methods. As shown in Fig. 2j, our stamp-patterned MoS_2 had a similar PL curve as the as-grown film (6,000 intensity and 670 nm peak), verifying that this dry-patterning process did not damage the 2D materials. By contrast, the traditional RIE-patterned samples had a decreased PL intensity (3,500 intensity) and a shifted PL peak (682 nm peak) due to residue or strain generation, which indicate that its optical properties had decreased due to the wet-patterning process. Subsequently, we randomly measured the PL spectra of 200 independent samples and performed a statistical analysis of the peaks and intensities (Fig. 2k,l). The stamp-patterned samples had better optical quality and higher uniformity than those produced by the traditional RIE method. Note that the original CVD MoS_2 films for the above two patterning methods were derived from one chip. The measurement parameters were kept constant for a fair comparison (see Methods for more details). Note that our stamp imprinting method could easily be extended to other 2D monolayers, such as CVD-grown WS_2, CVD-grown WSe_2 and exfoliated monolayer MoS_2 (Supplementary Fig. 9).

Uniformity of MoS_2 transistor arrays

With large-scale MoS_2 on SiO_2/Si substrate synthesized by CVD, we could directly pattern individual monolayer films and fabricate back-gated transistor arrays (see Methods for details). Figure 3a shows an optical image of large-scale transistor arrays. The semimetal bismuth (Bi) was used for the source and drain contact electrodes[38], and highly doped silicon and 280 nm of SiO_2 were used for the back gate. As shown in Fig. 3b,c, the I_{ds}–V_{gs} transfer curves (where I_{ds} is the drain–source current and V_{gs} is the gate-to-source voltage) show n-type behaviour and an on/off ratio of 10^8. The I_{ds}–V_{ds} output characteristics (where V_{ds} is the drain–source bias) show linear behaviour, indicating near ohmic contact between the source/drain metal and the monolayer MoS_2 channel. To systematically explore the uniformity, we characterized the electronic properties of 100 randomly selected MoS_2 transistors fabricated by our stamp-patterning and 100 devices fabricated by the traditional RIE method (as control samples) on one chip. Each device had the same channel length of 5 μm and width of 10 μm (Fig. 3d and Supplementary Fig. 10). Although all the transistors exhibited n-type conductive behaviour, the samples prepared by our stamp-patterning (red lines) had large advantages in terms of electronic performance and uniformity over the traditional RIE method (blue lines). Specifically, a histogram analysis of the threshold voltage (V_{th}, defined as where I_{ds} = 0.1 nA μm^{-1}) and nonlinear fitting with a Gaussian function (grey curve in Fig. 3e) demonstrated that V_{th} of the RIE devices (peak V_{th} = −46 V) was more negative and its variation spread (standard error

https://doi.org/10.1038/s41928-025-01408-z

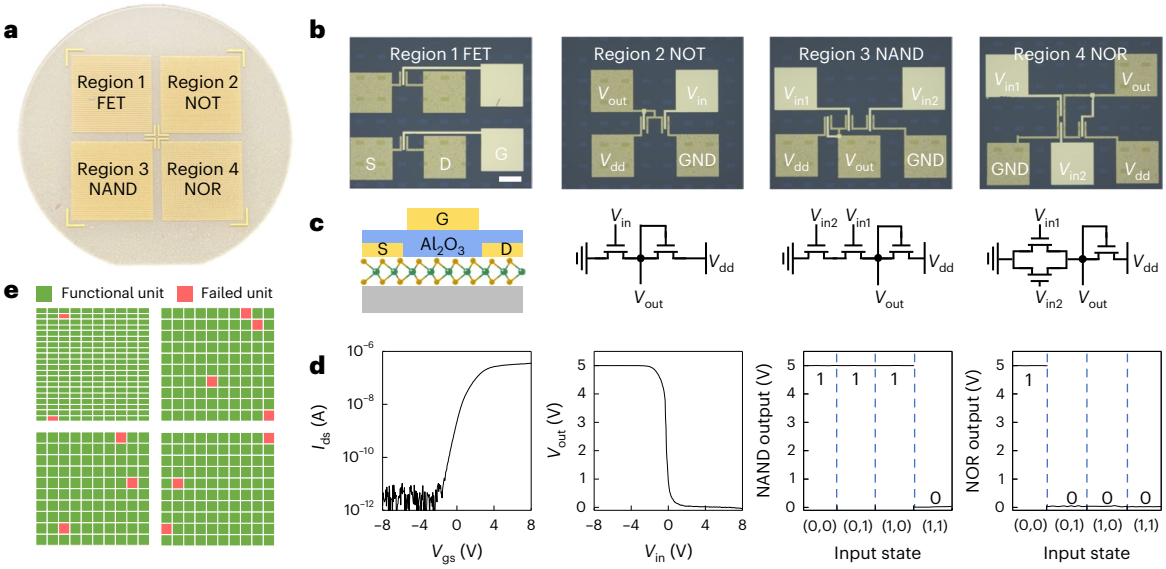

Fig. 4 | Wafer-scale logic circuits from stamp-patterned MoS_2 arrays. **a**, Photograph of a 2-inch wafer with a top-gated FET in region 1, NMOS NOT gate arrays in region 2, NAND gate arrays in region 3 and NOR gate arrays in region 4. **b**,**c**, Optical images (**b**) and schematics (**c**) of the top-gated FET and logic circuits. **d**, Transfer curve of the top-gated FET and the output voltage of the logic circuits with a power supply of V_{dd} = 5 V. **e**, Wafer yield map of 500 FET and logic-gate arrays. The green and red squares represent the functional and failed units, respectively. D, drain; S, source; G, gate; GND, ground; V_{dd}, drain supply voltage; V_{in}, input voltage; V_{out}, output voltage; V_{in1}, input voltage 1; V_{in2}, input voltage 2. Scale bar, 50 µm.

of Gaussian fitting, σ = 2.125) was about 20 times higher than that in our stamp-patterned MoS_2 devices (V_{th} = −28 V and σ = 0.108), which we largely attribute to the effects of doping and the uncontrollable quality degradation caused by polymer residues left by the traditional RIE process. Subsequently, we extracted and analysed the on/off ratio and carrier mobility (Fig. 3f). Our stamp-patterned devices exhibited high performance with a narrow distribution of the on/off ratio $I_{on}/I_{off} \approx 10^8$ (σ = 0.023) and mobility of 18.8 $cm^2 V^{-1} s^{-1}$ (σ = 0.542) (highlighted by the green area), whereas the control devices had lower values and a larger variation of $I_{on}/I_{off} \approx 10^6$ (σ = 0.158) and mobility of 7.5 $cm^2 V^{-1} s^{-1}$ (σ = 1.937) (highlighted by the orange area). The above comparison verified that our stamp-patterning method can better retain a residue-free and high-quality 2D crystal compared to the traditional RIE method, thus ensuring the fabrication of large-scale transistors with higher electrical performance and uniformity.

High yield of wafer-scale logic circuits

To demonstrate the potential of our metal-stamp-patterning method for industrial high-volume production, we fabricated a variety of basic logic circuit arrays on a 2-inch wafer with stamp-patterned MoS_2 (Fig. 4a). The wafer was divided into four functional areas: FET (region 1), n-type metal–oxide–semiconductor (NMOS) NOT (region 2), NAND (region 3) and NOR (region 4) logic gates (Fig. 4b,c). For the top-gated MoS_2 FET, the source/drain electrode (Bi/Au), top dielectric (Al_2O_3) and gate electrode (Cr/Au) were fabricated after MoS_2 channel patterning (see Methods for more details). The I_{ds}–V_{gs} transfer characteristic shows n-type behaviour. We fabricated the logic NOT gate by integrating two adjacent FETs. The device generated a low voltage (off state) when a positive voltage was loaded in input voltage (V_{in}), which became a high voltage (on state) when a negative voltage was loaded, achieving the NOT logic function. We fabricated the NAND and NOR logic gates by integrating more top-gated FETs, also achieving the correct logic functions and rail-to-rail conversion (Fig. 4d). Furthermore, we individually tested 200 top-gated FETs (region 1) and 300 logic gates (regions 2 to 4) on the wafer and obtained the device yield mapping. As shown in Fig. 4e, where the green and red squares represent functional and failed units respectively, we achieved a yield of functioning devices of 97.6% (488 units/500 units). The successful construction of basic logic gates shows that stamp-patterned 2D materials are suitable for various electronic circuits.

Conclusions

We have described a residue-free imprinting method for patterning wafer-scale 2D materials using a 3D metal stamp. The surface cleanness and optical quality of our stamp-patterned MoS_2 arrays—characterized with AFM, PL and STEM measurements—were consistent with those of as-grown intrinsic crystal films. We showed that the stamp-patterning method can be used to fabricate large-scale transistors and logic circuits, with higher performance, uniformity (20 times lower standard error for V_{th}) and yield (97.6%) compared to a traditional RIE patterning method. Our method provides a high-throughput patterning technology that overcomes the contamination issues associated with large-scale patterning of 2D materials by traditional methods, thus facilitating the production of uniform, high-yield electronic devices. Additionally, we anticipate that the arrays with intrinsically clean 2D surfaces and the edges obtained by this method will be conducive for research in fields such as twisted moiré superlattices[39,40], confined secondary growth[41,42], monolithic 3D integration[43–45] and 2D materials towards industrialization[46,47].

Methods

Metal-stamp fabrication and patterning process

First, photolithography was conducted on a polished Si wafer to pattern the mould structure, followed by the electron-beam deposition (or sputtering) of a SiO_2 film. The thickness of the film had to be greater than 300 nm to ensure the structure of our 3D stamp (counter to the previous 2D structure without dents[35,48]) and the subsequent patterning yield (Supplementary Fig. 11). The deposition rate was ~1 Å s^{-1}. We conducted the lift-off process in hot acetone (Fig. 1h and Supplementary Fig. 1a). Next, a 50-nm-thick Au film (thermal evaporation rate of ~0.5 Å s^{-1}) was deposited (Supplementary Fig. 1b), followed by spin-coating a 10 wt% poly(bisphenol A carbonate) layer (Aldrich; molecular weight ~45,000 g mol^{-1}) on the surface of the 3D SiO_2 mould with a speed of 3,000 rpm for 60 s and baked at 100 °C for 3 min. The Au and poly(bisphenol A carbonate) films were peeled from the Si substrate with PI tape plus a polydimethylsiloxane supporting layer

and flipped onto the surface of glass plus a metal frame to prepare the Au stamp (Supplementary Fig. 1c), which inherited the inverted 3D morphology of the prefabricated mould. Immediately, the 3D Au stamp was then pressed onto the surface of the as-grown 2D film and heated at 120 °C for 3–5 min. After separating the stamp, large-area MoS_2 arrays could be observed on the substrate. In addition, note that when the Au functional layer in the metal stamp was replaced by a cheaper metal Ag, we obtained the same 2D array with our imprinting method (Supplementary Fig. 12).

To fabricate control samples with a traditional RIE method, a photoresist (Micro Resist Technology, S1850) was spin-coated onto an as-grown 2D film with a speed of 6,000 rpm for 60 s and baked at 110 °C for 3 min, followed by photolithography to fabricate mask patterns. Next, RIE (O_2) was conducted to etch the samples (power of 50 W for 10 s), followed by soaking in hot acetone (60 °C for 1 h) to remove the photoresist mask and obtain MoS_2 arrays.

PL and Raman characterizations

The prepared samples were placed on a confocal microscope (WITEC Alpha 200R) to measure the Raman and PL spectra. For the PL spectrum measurement, a 532-nm laser with a 1,800 lines per millimetre grating was used. The laser power was 0.6 mW. For the Raman spectrum measurement, a 532-nm laser was used with 1 mW power and a grating level of 2,400 lines per millimetre.

Fabrication of monolayer MoS_2 FET arrays

After patterning MoS_2 arrays on a grown SiO_2/Si substrate (dielectric/back gate), photolithography was conducted to pattern the source and drain electrodes (maskless ultraviolet lithography, TuoTuo Technology Co, Ltd), followed by the deposition of Bi/Au (20 nm of Bi and 50 nm of Au) using a thermal evaporation system under vacuum (pressure ~10^{-7} Torr) and lift-off. For fair comparison, the original CVD MoS_2 films for the two patterning methods were derived from one chip. The device fabrication and measurement parameters were kept constant.

Fabrication of wafer-scale logic circuits

After patterning MoS_2 arrays on a grown 2-inch sapphire substrate, first, photolithography was conducted to pattern the source and drain electrodes, followed by deposition of Bi/Au (20 nm of Bi and 30 nm of Au) and lift-off. Next, we used atomic layer deposition to deposit a high-κ gate dielectric (20 nm of Al_2O_3) at 150 °C using trimethyl aluminium and water as precursors. The via of the gate dielectric layer was created by a second photolithography step and solution-etching of Al_2O_3 by NaOH. Last, a third photolithography step was conducted to pattern the top-gate electrodes, followed by deposition of Cr/Au (2 nm of Cr and 50 nm of Au) and lift-off. The electronic measurements of the wafer-scale logic gates were conducted in air using a semiconductor analyser (Keithley 4200A).

Atomistic modelling

Atomistic modelling was performed using a universal neural network interatomic potential, the preferred potential, which is a measure of the total energy and forces on atoms for a given atomic configuration. We incorporated D3 corrections to account for interactions. The MoS_2/substrate interface was modelled as a slab consisting of 8 × 8 Au(111) and 4 × 4 Al_2O_3(0001) layers, each with a thickness greater than 10 Å. A single layer of 6 × 6 MoS_2(0001) was adsorbed on one side of the slab, with a vacuum region of 25 Å included to prevent interactions with periodic images. The positions of the atoms were allowed to relax until the force on each atom was smaller than 0.005 eV/Å and the difference in potential energy between successive iterations was less than 0.01 eV. The adhesion energy ($E_{adhesion}$) was calculated using the following expression: $E_{adhesion} = E_{sub} + E_{MoS_2} - E_{sub/MoS_2}$, where E_{sub}, E_{MoS_2} and E_{sub/MoS_2} represent the potential energies of the substrate (Au or Al_2O_3), the MoS_2 layer and the combined substrate/MoS_2 slab, respectively. To account for strain energy resulting from lattice mismatch, the combined structures were optimized first, and the cell parameters were fixed during the relaxation of the individual Al_2O_3, Au and MoS_2 slabs.

Data availability

Data that support the plots within this paper and other findings of this study are available from the corresponding authors on reasonable request. Source data are provided with this paper.

References

1. Chhowalla, M., Jena, D. & Zhang, H. Two-dimensional semiconductors for transistors. *Nat. Rev. Mater.* **1**, 16052 (2016).
2. Qiu, H. et al. Two-dimensional materials for future information technology: status and prospects. *Sci. China Inf. Sci.* **67**, 160400 (2024).
3. International Roadmap Committee. *International Roadmap for Devices and Systems* (IEEE, accessed 2023); https://irds.ieee.org/
4. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
5. Liu, Y., Huang, Y. & Duan, X. Van der Waals integration before and beyond two-dimensional materials. *Nature* **567**, 323–333 (2019).
6. Li, W. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
7. Tan, C. et al. 2D fin field-effect transistors integrated with epitaxial high-*k* gate oxide. *Nature* **616**, 66–72 (2023).
8. Xia, Y. et al. 12-inch growth of uniform MoS_2 monolayer for integrated circuit manufacture. *Nat. Mater.* **22**, 1324–1331 (2023).
9. Li, T. et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* **16**, 1201–1207 (2021).
10. Qin, B. et al. Interfacial epitaxy of multilayer rhombohedral transition-metal dichalcogenide single crystals. *Science* **385**, 99–104 (2024).
11. Liu, L. et al. Transferred van der Waals metal electrodes for sub-1-nm MoS_2 vertical transistors. *Nat. Electron.* **4**, 342–347 (2021).
12. Li, W. et al. Monolayer black phosphorus and germanium arsenide transistors via van der Waals channel thinning. *Nat. Electron.* **7**, 131–137 (2023).
13. Pham, P. et al. 2D heterostructures for ubiquitous electronics and optoelectronics: principles, opportunities, and challenges. *Chem. Rev.* **122**, 6514–6613 (2022).
14. Min-Dianey, K., Le, T., Choi, J. & Pham, P. Advanced optical detection through the use of a deformably transferred nanofilm. *Nanomaterials* **11**, 816 (2021).
15. Liu, S. et al. Nanopatterning technologies of 2D materials for integrated electronic and optoelectronic devices. *Adv. Mater.* **34**, e2200734 (2022).
16. Mondal, A. et al. Low ohmic contact resistance and high on/off ratio in transition metal dichalcogenides field-effect transistors via residue-free transfer. *Nat. Nanotechnol.* **19**, 34–43 (2024).
17. Zhao, Y. et al. A clean transfer approach to prepare centimetre-scale black phosphorus crystalline multilayers on silicon substrates for field-effect transistors. *Nat. Commun.* **15**, 6795 (2024).
18. Nakatani, M. et al. Ready-to-transfer two-dimensional materials using tunable adhesive force tapes. *Nat. Electron.* **7**, 119–130 (2024).
19. Shu, Z. et al. Near-zero-adhesion-enabled intact wafer-scale resist-transfer printing for high-fidelity nanofabrication on arbitrary substrates. *Int. J. Extreme Manuf.* **6**, 015102 (2024).
20. Pham, P. et al. Transfer of 2D films: from imperfection to perfection. *ACS Nano* **18**, 14841–14876 (2024).
21. Mao, H., Wu, D., Wu, W., Xu, J. & Hao, Y. The fabrication of diversiform nanostructure forests based on residue nanomasks synthesized by oxygen plasma removal of photoresist. *Nanotechnology* **20**, 445304 (2009).

22. Franquet, A. et al. Characterization of post-etched photoresist and residues by various analytical techniques. *Appl. Surf. Sci.* **255**, 1408–1411 (2008).
23. Choi, A. et al. Residue-free photolithographic patterning of graphene. *Chem. Eng. J.* **429**, 132504 (2022).
24. Poddar, P. K. et al. Resist-free lithography for monolayer transition metal dichalcogenides. *Nano Lett.* **22**, 726–732 (2022).
25. Garcia, R., Knoll, A. W. & Riedo, E. Advanced scanning probe lithography. *Nat. Nanotechnol.* **9**, 577–587 (2014).
26. Albisetti, E. et al. Thermal scanning probe lithography. *Nat. Rev. Methods Primers* **2**, 32 (2022).
27. Wei, Z. et al. Scratching lithography for wafer-scale MoS_2 monolayers. *2D Mater.* **7**, 045028 (2020).
28. Hummel, A. W. Movable type printing in China: a brief survey. *Q. J. Curr. Acquis.* **1**, 18–24 (1944).
29. Maruyama, N. et al. Advances and applications in nanoimprint lithography. In *Proc. Novel Patterning Technologies 2023* 124970D (SPIE, 2023).
30. Asano, T. et al. The advantages of nanoimprint lithography for semiconductor device manufacturing. In *Proc. SPIE 11178* 111780I (SPIE, 2019).
31. Huang, Y. et al. Universal mechanical exfoliation of large-area 2D crystals. *Nat. Commun.* **11**, 2453 (2020).
32. Liu, F. et al. Disassembling 2D van der Waals crystals into macroscopic monolayers and reassembling into artificial lattices. *Science* **367**, 903–906 (2020).
33. Ding, S. et al. Ag-assisted dry exfoliation of large-scale and continuous 2D monolayers. *ACS Nano* **18**, 1195–1203 (2024).
34. Fu, Q. et al. One-step exfoliation method for plasmonic activation of large-area 2D crystals. *Adv. Sci.* **9**, e2204247 (2022).
35. Li, Z. et al. Dry exfoliation of large-area 2D monolayer and heterostructure arrays. *ACS Nano* **15**, 13839–13846 (2021).
36. Kim, K. et al. van der Waals heterostructures with high accuracy rotational alignment. *Nano Lett.* **16**, 1989–1995 (2016).
37. Cao, Y. et al. Tunable correlated states and spin-polarized phases in twisted bilayer-bilayer graphene. *Nature* **583**, 215–220 (2020).
38. Shen, P. C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
39. Lian, Z. et al. Valley-polarized excitonic Mott insulator in WS_2/WSe_2 moiré superlattice. *Nat. Phys.* **20**, 34–39 (2024).
40. Tan, Q. et al. Layer-dependent correlated phases in WSe_2/MoS_2 moiré superlattice. *Nat. Mater.* **22**, 605–611 (2023).
41. Kim, K. S. et al. Non-epitaxial single-crystal 2D material growth by geometric confinement. *Nature* **614**, 88–94 (2023).
42. Li, J. et al. General synthesis of two-dimensional van der Waals heterostructure arrays. *Nature* **579**, 368–374 (2020).
43. Lu, D. et al. Monolithic three-dimensional tier-by-tier integration via van der Waals lamination. *Nature* **630**, 340–345 (2024).
44. Guo, Y. F. et al. Van der Waals polarity-engineered 3D integration of 2D complementary logic. *Nature* **630**, 346–352 (2024).
45. Jayachandran, D. et al. Three-dimensional integration of two-dimensional field-effect transistors. *Nature* **625**, 276–281 (2024).
46. Kim, K. S. et al. The future of two-dimensional semiconductors beyond Moore's law. *Nat. Nanotechnol.* **19**, 895–906 (2024).
47. Milana, S. The lab-to-fab journey of 2D materials. *Nat. Nanotechnol.* **14**, 919–921 (2019).
48. Satterthwaite, P. et al. Van der Waals device integration beyond the limits of van der Waals forces using adhesive matrix transfer. *Nat. Electron.* **7**, 17–28 (2024).

Acknowledgements

This work is supported by A*STAR (Grant Nos. M21K2c0116 and M24M8b0004), the Singapore National Research Foundation (Grant Nos. NRF-CRP22-2019-0004, NRF-CRP30-2023-0003, NRF2023-ITC004-001 and NRF-MSG-2023-0002) and the Singapore Ministry of Education (MOE) Tier 2 Grant (Grant No. MOE-T2EP50222-0018). H.C. acknowledges the support from the robotic AI-Scientist platform of Chinese Academy of Sciences and Anhui Outstanding Young Scientist Fund (2408085J005). Z. Liu acknowledges the support from the National Research Foundation, Singapore, under its Competitive Research Programme (CRP) (NRF-CRP22-2019-0007). This work is also supported by A*STAR MTC Programmatic Grant M23M2b0056. T.L. acknowledges the support from the National Natural Science Foundation of China (grant nos. 62322408 and 62204113). X.R.W. acknowledges support from the Singapore MOE Academic Research Fund (AcRF) Tier 3 (Grant No. MOE-MOET32023-0003) 'Quantum Geometric Advantage' and Tier 1 (Grant Nos. RG82/23 and RG155/24).

Author contributions

W.G. and Z. Li conceived the project. Z. Li performed the experiments and data analysis. X.L. contributed to the PL and transistor measurements. J.S. contributed to the photolithography and logic-gate fabrication. X.C. contributed to the STEM characterization. Y.Z. contributed to drawing the schematics. W.C., Y.J., H.J., C.Z., Y.D., Y.L., X.R.W., H.C. and Z. Liu contributed to device fabrication. S.Y.K. and J.L. contributed to the atomistic modelling. T.L. provided the wafer monolayer MoS_2 film. W.G. and Z. Li co-wrote the paper. All authors discussed the results and commented on the paper. Z. Li and X.L. contributed equally to this work.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-025-01408-z.

Correspondence and requests for materials should be addressed to Hongbing Cai or Weibo Gao.

Peer review information *Nature Electronics* thanks Huigao Duan, Phuong V. Pham and Yanbo Xie for their contribution to the peer review of this work.