NANO LETTERS

Letter

pubs.acs.org/NanoLett

All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor

Saptarshi Das,*[,†,‡] Richard Gulotty,[†,§] Anirudha V. Sumant,*[,†] and Andreas Roelofs[†]

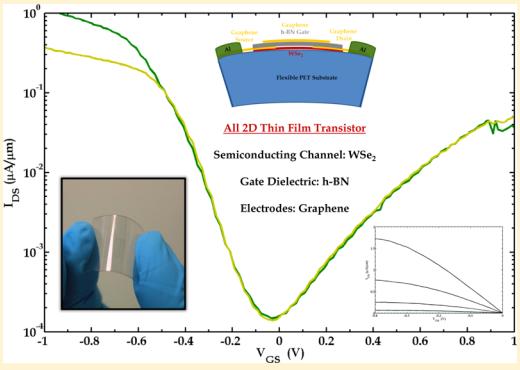
[†]Center for Nanoscale Material, Argonne National Laboratory, Argonne, Illinois 60439, United States

[‡]Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States

[§]Materials Science and Engineering Program, Bourns College of Engineering, University of California − Riverside, Riverside, California 92521 United States

Supporting Information

ABSTRACT: In this article, we report only 10 atomic layer thick, high mobility, transparent thin film transistors (TFTs) with ambipolar device characteristics fabricated on both a conventional silicon platform as well as on a flexible substrate. Monolayer graphene was used as metal electrodes, 3−4 atomic layers of h-BN were used as the gate dielectric, and finally bilayers of WSe_2 were used as the semiconducting channel material for the TFTs. The field effect carrier mobility was extracted to be 45 $cm^2/(V\ s)$, which exceeds the mobility values of state of the art amorphous silicon based TFTs by ∼100 times. The active device stack of WSe_2−hBN−graphene was found to be more than 88% transparent over the entire visible spectrum and the device characteristics were unaltered for in-plane mechanical strain of up to 2%. The device demonstrated remarkable temperature stability over 77−400 K. Low contact resistance value of 1.4 kΩ-μm, subthreshold slope of 90 mv/decade, current ON−OFF ratio of 10^7, and presence of both electron and hole conduction were observed in our all two-dimensional (2D) TFTs, which are extremely desirable but rarely reported characteristics of most of the organic and inorganic TFTs. To the best of our knowledge, this is the first report of all 2D transparent TFT fabricated on flexible substrate along with the highest mobility and current ON−OFF ratio.



KEYWORDS: *2D Crystal, graphene, thin film transistor, flexible electronics*

Two dimensional (2D) layered materials like graphene, hexagonal boron nitride (h-BN), and transition metal dichalcogenides (TMDs) are receiving significant attention across all scientific disciplines due to their unique electrical, mechanical, thermal, and optical properties.[1−12] High carrier velocity, exceptional mechanical stability, and near invisibility of graphene had already resulted in its commercialization as stretchable and transparent electrodes and interconnects.[1−4] Graphene has also been substantially investigated as an alternative to silicon for beyond CMOS nanoelectronics. However, the absence of a sizable bandgap prevents the use of graphene in the logic circuits and has paved the way for the exploration of semiconducting TMDs like MoS_2, WSe_2, $MoSe_2$, among others. Several high-performance field effect transistors (FETs) based on TMDs have been demonstrated in the recent literature.[7−12] Various studies also indicate the potential of TMDs for optical, mechanical, chemical, and thermal applications.[13−17] Finally, h-BN complements both, highly conductive graphene and semiconducting TMDs, not only by being a large bandgap insulator, but also, often as a substrate with better interface qualities.[5,6] Integrating the unique properties of these different 2D materials therefore provides numerous possibilities to shape the future of nanoelectronics.

One of the most promising applications of optimally stacked 2D materials is as thin film transistors (TFT). The recent outburst of the display technology has made it even more appealing because the light emitting diodes (LEDs) and liquid crystal displays (LCDs) are driven by TFTs. TFTs are also used in RFID tags, flexible electronic devices, and for sensing applications. Although, the thin film transistor industry is reasonably mature, it is nowhere close to the ultimate potential due to limited material choices. Amorphous silicon (a-Si) is the most popular and widely used material for the TFTs.[18,19] Numerous organic and inorganic materials had also been extensively explored.[20−23] However, search for the better materials is still on. The most desirable features of TFTs are high carrier mobility, high ON−OFF current ratio, low contact resistance, presence of both electron and hole conduction, high optical transparency, temperature stability, and mechanical flexibility.[24] The 2D layered materials are a natural choice for the TFTs in order to meet these requirements. Moreover, their inherent electrostatic integrity allows them to operate at low

Received: March 10, 2014
Revised: April 15, 2014
Published: April 22, 2014

   dx.doi.org/10.1021/nl5009037 | *Nano Lett.* 2014, 14, 2861−2866

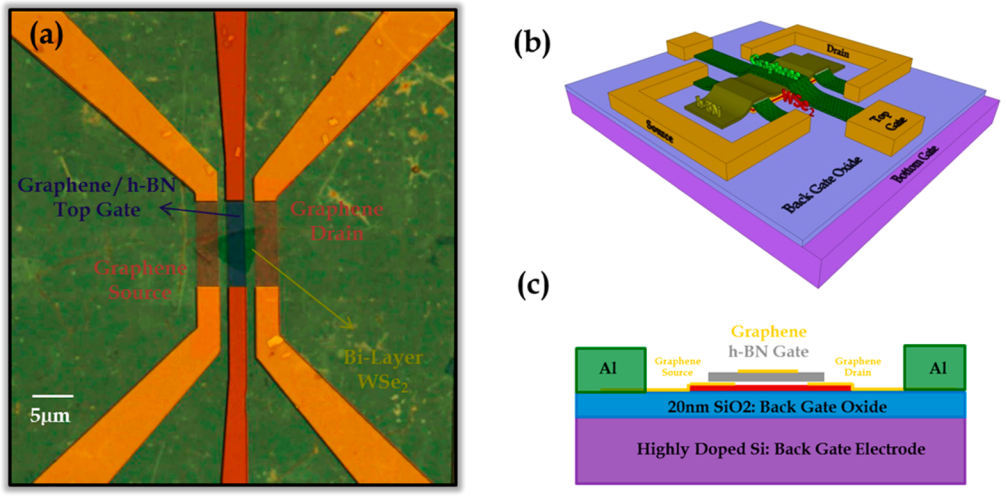


Figure 1. (a) False color SEM image (b) 3D cartoon, and (c) cross sectional view of an all 2D TFT with graphene as metal electrode, h-BN as gate dielectric and WSe_2 as the semiconducting channel material.

power and also make them more scalable. In this article, we experimentally demonstrate all 2D TFTs with monolayer graphene as metal electrodes, 3−4 atomic layers of h-BN as the gate dielectric and bilayers of WSe_2 as the semiconducting channel material. We extracted electron mobility of 34 $cm^2/(V\ s)$ and hole mobility of 45 $cm^2/(V\ s)$ that exceed the conventional a-Si mobility (0.5−1 $cm^2/(V\ s)$) by a factor of ∼100.[24] The current ON−OFF ratio was found to be more than 10^7. We also report low contact resistance of 1.4 kΩ-μm. When fabricated on flexible polyethylene terephthalate (PET) substrate, our active device stack of WSe_2−hBN−graphene was found to be more than 88% transparent over the entire visible spectrum and the device characteristics were unaltered for in-plane mechanical strain of up to 2%. The device also demonstrated temperature stability over 77−400 K.

Fabrication of TFTs on silicon platforms as well as on flexible polyethylene terephthalate (PET) substrates involved similar process flows. WSe_2 flakes were micromechanically exfoliated using standard scotch tape technique while large area chemical vapor deposition grown monolayer graphene and few layer h-BN were transferred on to the desired substrate. Optical lithography and reactive ion etching (RIE) were used for patterning purposes and electron beam evaporation was used for contact pads metallization (see the Supporting Information for the detailed fabrication process flow). Figure 1a shows the false color SEM image of an all 2D TFT on 20 nm SiO_2 substrate with highly doped Si as the back gate. Figure 1b,c, respectively, shows the three-dimensional cartoon and the cross sectional view of our device.

Figure 2a shows the back-gated transfer characteristics of an all 2D TFT with bilayer WSe_2 flake as the channel material and graphene as the source/drain contact electrodes. Note that all the graphene electrodes are connected to metal pads at both ends to ensure uniform potential landscape across the entire graphene contacts (Figure 1b). An interesting feature of graphene contact is that, unlike conventional metal electrodes, the Fermi level of graphene responds to the back gate bias in spite of the charge screening by the WSe_2 channel underneath the contacts. Figure 2b shows the transfer characteristics of a graphene field effect transistor (GFET) with underlying WSe_2 as the screening layer. The characteristic is very similar to conventional GFET devices which clearly suggest that the underlying WSe_2 acts as just an additional dielectric layer. Figure 2c shows the position of the Fermi level inside graphene in response to the applied back gate bias screened by bilayer WSe_2. We have used the Landauer formalism for current transport and taken into account the quantum capacitance contribution in order to solve the self-consistent Poisson equation to calculate $\Psi_{GRAPHENE}$. The details can be found elsewhere.[25−27] Our numerical calculations backed by experimental observations suggest that the Fermi level in graphene can be moved by ∼300 meV on either side of the Dirac point over the applied gate bias range.[28,29] This is an important finding in the context of graphene to WSe_2 contact as will be discussed next.

The presence of both the electron and the hole conduction in our WSe_2 thin film transistor (Figure 2a) strongly suggests that the Dirac point of graphene aligns close to the middle of the bandgap of WSe_2. Because the bandgap of bilayer WSe_2 is ∼1.3 eV, this would indicate the existence of large Schottky barrier heights at graphene to WSe_2 contacts for both electron injection into the conduction band (Φ_{N0}) and hole injection into the valence band (Φ_{P0}) as shown in the associated band diagram in Figure 2d (brown box). When a negative gate bias is applied, the energy bands in WSe_2 bend to facilitate hole injection into the valence band and at the same time the Fermi level in graphene also moves closer to the valence band, thereby reducing the effective Schottky barrier height for hole injection to Φ_P as shown in the purple box in Figure 2d. Similarly for positive gate bias, the energy bands in WSe_2 bend to facilitate electron injection into the conduction band and at the same time the Fermi level in graphene also moves closer to the conduction band, thereby reducing the effective Schottky barrier height for electron injection to Φ_N as shown in the black box in Figure 2d. Using the technique proposed by Das[11] and adjusting the effective bandgap of WSe_2 to take into account the band movement in graphene, the height of the Schottky barrier at the graphene-to-WSe_2 contact was extracted to be 0.38 eV for the electron injection into the conduction band and 0.22 eV for the hole injection into the valence band at threshold bias condition. Figure 2e,f shows the partially top-gated transfer characteristics of the same TFT with h-BN as the gate dielectric and graphene as the gate electrode corresponding to two different biasing condition of the back gate, V_{BG} = 10 V and V_{BG}

dx.doi.org/10.1021/nl5009037 | Nano Lett. 2014, 14, 2861−2866

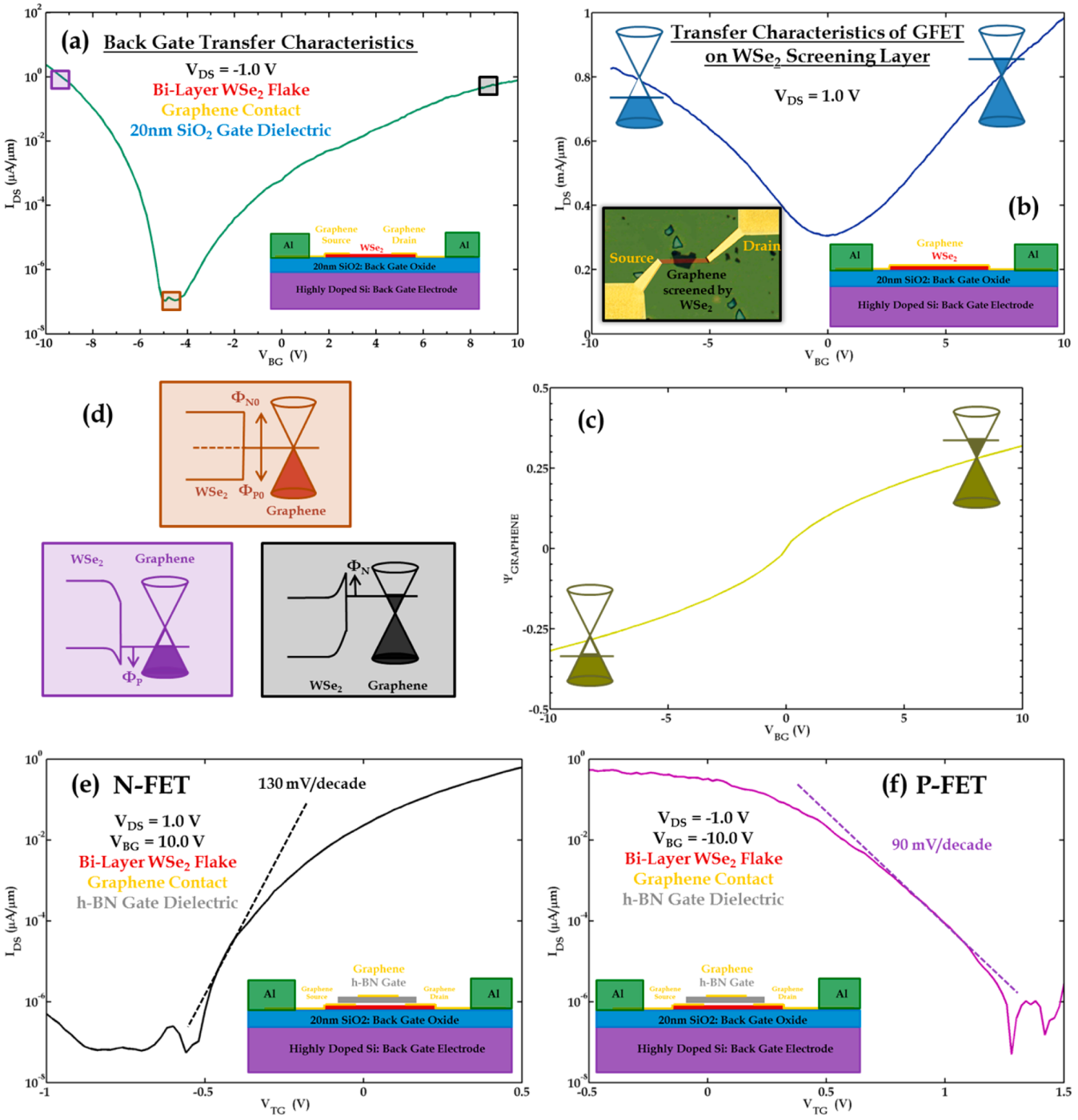


Figure 2. (a) Back gate transfer characteristics of a WSe_2TFT with graphene as contact electrodes. Inset shows the cross section of the device. (b) Back gate transfer characteristics of a graphene FET with underlying WSe_2 screening layer. Inset shows the false color SEM image and the cross section of the device. (c) Band movement ($\Psi_{GRAPHENE}$) in graphene in response to applied back gate bias. (d) Band alignment at graphene to WSe_2 contact interface at different back gate bias conditions shown in (a). (e,f) Top gate transfer characteristics of all 2D TFT corresponding to two different back gate biases, V_{BG} = 10 V and V_{BG} = −10 V, respectively.

= −10 V respectively. For negative back gate biases, the WSe_2 flake is electrostatically p-doped and hence the top gated device exhibits p-FET characteristics, while for positive back gate biases the WSe_2 flake is electrostatically n-doped and hence the top gated device exhibits n-FET characteristics. The subthreshold slope was found to be ∼90 mV/decade for the p-FET and ∼130 mV/decade for the n-FET.

The field effect mobility values were extracted using the conventional equation for $g_m = \mu C_{OX}(W/L)V_{DS}$ (where g_m is the trans-conductance, μ is the field effect mobility, and W and L are the channel width and the channel length, respectively, $C_{OX} = \varepsilon_{OX}/d_{OX}$, where ε_{OX} is the dielectric constant and d_{OX} is the thickness of the gate oxide, d_{OX} = 3 nm and for h-BN, $\varepsilon_{OX} = 6 \times 10^{-11}$, which gives $C_{OX} \sim 3.10^{-2}$ F/m^2, and finally $L \sim 5$ μm) from the back-gated device characteristics. The field-effect mobility values were found to be 24 and 45 cm^2/(V s) for electrons and holes, respectively. The reader should note that the mobility of amorphous Si is in the range of 0.5−1 cm^2/(V

dx.doi.org/10.1021/nl5009037 | Nano Lett. 2014, 14, 2861−2866

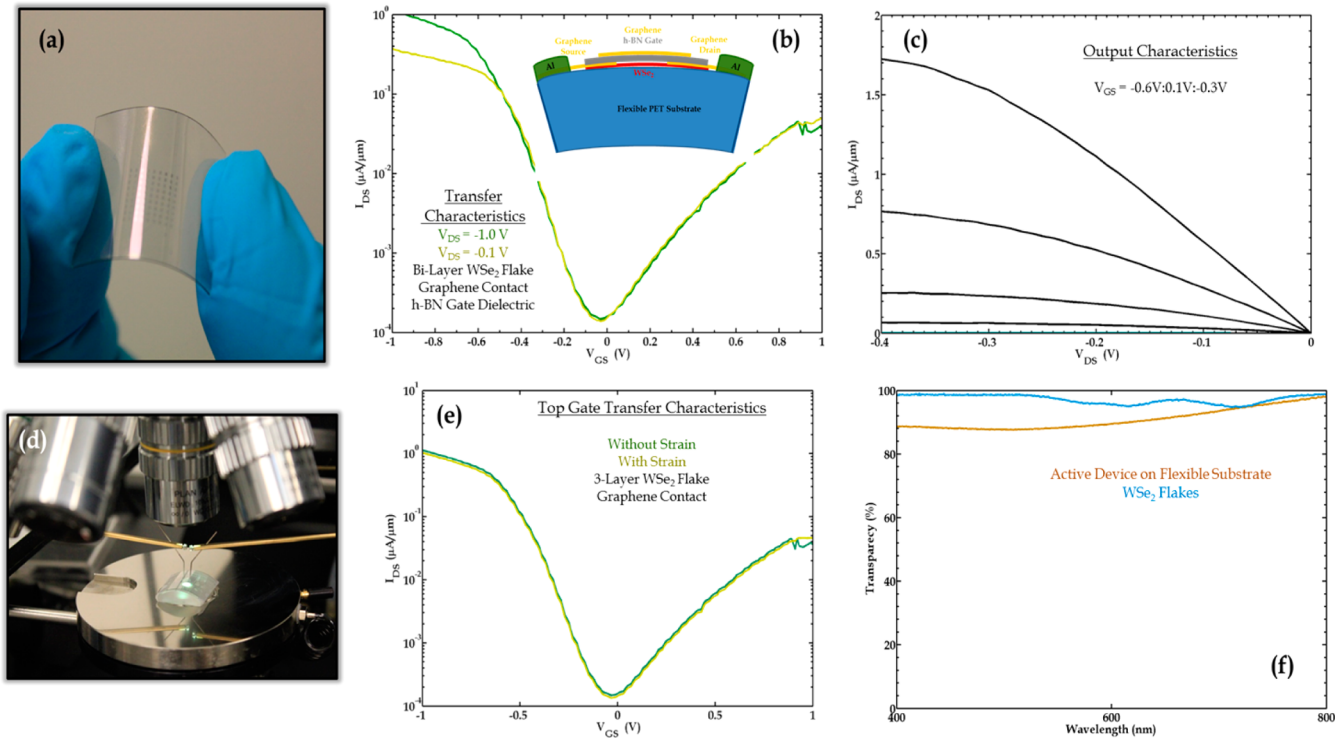


Figure 3. (a) Thinnest field effect transistor on flexible PET substrate. (b) Transfer characteristics and (c) output characteristics of the TFT. (d) Experimental setup to measure the strain effect. (e) Device characteristics under strain and (f) transparency of the TFT and its individual components.

s) while the mobility of most of the organic semiconductors is <1 $cm^2/(V\ s)$.[20,24] Our mobility values therefore out perform the state of the art TFT technologies by ∼2 orders of magnitude. Metal oxide semiconductors like indium tin oxide, ZnO, and most recently alloys like InGaZnO had demonstrated mobility values as high as 1−100 $cm^2/(V\ s)$ but the oxide TFTs suffer significantly from threshold voltage shift and hence electrical instability due to doping created by oxygen vacancies.[22−24] Our all 2-D TFTs show remarkable threshold voltage stability when measured in vacuum and air as well as over a span of time. Nanowire and carbon nanotube based TFTs had also demonstrated mobility values in the range of 10−100 $cm^2/(V\ s)$.[30,31] However, the placement of the wires/tubes and the variability in their transport properties depending on their dimensions (diameters) and connectivity (percolation path in a film) are major challenges in the realization of TFTs using these materials. The fact that the 2D materials can be grown over large area eliminates the placement problem and at the same time their natural sheet like structure keeps the diffusive transport models applicable in order to benchmark their performance limits.

The drive current (I_{DRIVE}) is another important parameter for the TFTs in the context of LEDs and LCDs. Depending upon the material and the desired brightness, a single pixel of an organic LED requires 1−10 μA of current. Note that this drive current is easily achieved in our all 2D TFTs at a drive voltage of as low as $V_{DS} = V_{GS} = 1$ V. Also note that our experimental prototype device is not scaled properly (channel lengths are in several micrometers). A properly scaled device can have much higher drive current densities at even lower voltages. This will allow reduction of active device area for the TFTs. Moreover, a single TFT can potentially drive several LEDs, which will reduce cost, power dissipation, as well as open up avenues for innovative circuit design.

The drive current is also important in the context of LCDs. The charging time of a pixel is inversely proportional to the drive (charging) current ($\tau = V_{DD}C_{PIXEL}/I_{DRIVE}$, where τ is the charging time, V_{DD} is the supply voltage, and C_{PIXEL} is the pixel capacitance). For a standard pixel capacitance in the range of 0.1−1pF, our all 2D TFTs will have a charging time of 0.1−1 μs. The resolution of an LCD ($\beta = V_{DD}C_{PARA}/C_{PIXEL}$, where C_{PARA} is the parasitic capacitance) can also be significantly enhanced by using our all 2D TFT. For a standard parasitic capacitance of 50 fF, resolution of 5−50 mV can be achieved. Finally a figure of merit ($\gamma = \tau^{-1}\beta^{-1}$) as high as 10^8−10^{10} can be obtained which is 2−4 orders of magnitude higher than the state of the art a-Si TFTs.

One of the major reasons for fabricating our all 2D TFT on silicon platform is to demonstrate high degree of compatibility with the conventional CMOS technology. As the fundamental limitations do not allow Si to scale below 10 nm technology node without compromising sevelry on the device performance, low-dimensional materials, especially 2D semiconducting transistion metal dichalcogenides (TMDs) will become more and more relevant in the context of high-performance CMOS as well. Our earlier studies related to channel length scaling, good quality contact formation, and layer thickness optimization of TMDs has shown a lot of promise.[32−35] We have also implemented low power device concepts like tunneling FETs with the TMDs. There is a widespread concern about the low mobility values of the TMDs impacting the ON state performance of FETs.[36] However, one should remember that for technology nodes beyond 10 nm the devices will be dominated by ballistic transport and hence the more important parameters are going to be the carrier injection velocity and

dx.doi.org/10.1021/nl5009037 | Nano Lett. 2014, 14, 2861−2866

density of conducting modes. While carrier injection velocity of the TMDs are very similar to Si, the number of conducting modes for the TMDs far exceed Si due to their large effective masses (by a factor of 2−3) .[37] Moreover, the quantum effects (mostly reflected in increasing the bandgap of Si) will be absent when the channel thickness is scaled down for the TMDs. One of the major concerns for scaled transistors based on low-dimensional materials is the nonscalability of contact resistance due to finite transfer length and schottky barrier at the interface with the metal electrode. In this article, we have clearly demonstrated that such contact reistance values can be significantly reduced by using graphene as the electrode material.

Finally, Figure 3a shows our all 2D thin film transistors fabricated on a flexible PET substrate. Flexible electronics is another burgeoning industry with a lot of promise. The fact that most of the 2D materials are mechanically stable make them the natural choice for flexible electronics. Figure 3b,c shows the transfer and output characteristics of fully top gated device (note that the TFTs on flexible substrates do not have any back-gate and therefore require overlap of the gate electrode with the source/drain electrodes in order to eliminate access resistance to the channel. The contact resistance values for the p-FET was extracted to be 1.4 kΩ-μm for a gate overdrive voltage of $V_{GS} - V_{TH} = 1.0$ V. The contact resistance was calculated based on the extracted Schottky barrier height and the band bending length λ by using Landauer formula for current transport. The low values for contact resistances are extremely encouraging. The reader might be surprised about the numbers given that the heights of the Schottky barriers (Φ_P = 0.22 eV) at the graphene-to-WSe_2 contacts are significantly large. However, it should be noted that in a Schottky barrier field effect transistor the ON-state current is dominated by tunneling through the barrier. The fact that we are using 3 nm h-BN (EOT = 1.8 nm) as the gate dielectric and 1.5 nm WSe_2 flake as the channel material, results in a tunneling distance of λ = 1.6 nm, which makes the barrier almost transparent to the charge carriers.[35] The tunneling distance λ is calculated as the geometric mean of the oxide thickness and channel thickness in an ultrathin geometry like ours. The subthreshold slope was found to be ∼180 mV/decade for the hole branch and ∼340 mV/decade for the electron branch. The device characteristics were also measured with and without strain using an arrangement shown in Figure 3d. It was encouraging to find that the device characteristics were unaltered even with 2% in-plane mechanical strain as shown in Figure 3e. It is difficult to confirm the invariability of the material properties (more specifically the electronic band structure of WSe_2) as a function of strain from this experiment because it is well known that most of the 2D materials have weak adhesion to the substrates and therefore could slide under strain. Finally, we measured the absorbance of visible light for the all 2D thin film transistor and found that it is ∼88% transparent over the entire spectrum. The absorbance of WSe_2 flakes was found to be less than 5%.

In the conclusion, we have experimentally demonstrated the thinnest, high performance, flexible, and transparent thin film transistor fabricated using only two-dimensional layered materials for the first time. Our all 2D TFT outperforms the state of the art a-Si TFT in mobility, drive current capability, and charging time. We have also extracted very low contact resistance values and subthreshold slopes. The presence of both electron and hole conduction is another unique feature of our all 2D TFTs. This work clearly shows the great potential of 2D electronics in shaping the future of thin film transistors.

■ ASSOCIATED CONTENT

Supporting Information

Fabrication process flow for all 2D thin film transistors. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: (S.D.) das.sapt@gmail.com; das@anl.gov.
*E-mail: (A.V.S.) sumant@anl.gov.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

Use of the Center for Nanoscale Materials was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-06CH11357.

■ REFERENCES

(1) Palacios, T. Graphene electronics: thinking outside the silicon box. *Nat. Nanotechnol.* **2011**, *6*, 464−5.
(2) Geim, A. K.; Novoselov, S. K. The rise of graphene. *Nat. materials* **2007**, *6*, 183−91.
(3) Bae, S.; Kim, H.; Lee, Y.; Xu, X.; Park, J.; Zheng, Y.; Balakrishnan, J.; Lei, T.; Kim, H. R.; Song, Y.; et al. Roll-to-roll production of 30-in. graphene films for transparent electrodes. *Nat. Nanotechnol.* **2010**, *5*, 574−578.
(4) Chen, X.; Akinwande, D.; Lee, K.; Close, G. F.; Yasuda, S.; Paul, B. C.; Fujita, S.; Kong, J.; Wong, H. P. Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics. *IEEE Trans. Electron Device* **2010**, *11*, 3137−3143.
(5) Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Wantabe, T.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J. Boron Nitride Substrate for high quality graphene electronics. *Nat. Nanotechnol.* **2010**, *5*, 722−726.
(6) Lee, K. H.; Shin, H.; Lee, J.; Lee, I.; Kim, G.; Choi, J. Y.; Kim, S. Large-Scale Synthesis of High-Quality Hexagonal Boron Nitride Nanosheets for Large-Area Graphene Electronics. *Nano Lett.* **2012**, *12*, 714−18.
(7) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−50.
(8) Das, S.; Chen, H.; Penumacha, A. V.; Appenzeller, J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **2013**, *13*, 100−5.
(9) Wang, H.; Yu, L.; Lee, Y.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.; Dubey, M.; Kong, J.; Palacios, T. Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **2012**, *12*, 4674−80.
(10) Podzorov, V.; Garshenson, M. E.; Kloc, Ch.; Zeis, R.; Bucher, E. High-mobility field-effect transistors based on transition metal dichalcogenides. *Appl. Phys. Lett.* **2004**, *84*, 3301.
(11) Das, S.; Appenzeller, J. WSe_2 field effect transistors with enhanced ambipolar characteristics. *Appl. Phys. Lett.* **2013**, *103*, 103501.
(12) Larentis, S.; Fallahazad, B.; Tutuc, E. Field-effect transistors and intrinsic mobility in ultra-thin $MoSe_2$ layers. *Appl. Phys. Lett.* **2012**, *101*, 223104.
(13) Splendiani, A.; Sun, L.; Zhang, Y.; Li, T.; Kim, J.; Chim, C.; Galli, G.; Wang, F. Emerging Photo-luminescent in Monolayer MoS_2. *Nano Lett.* **2010**, *10*, 1271−75.
(14) Eda, G.; Yamaguchi, H.; Voiry, D.; Fujita, T.; Chen, M.; Chhowalla, M. Photoluminescence from Chemically Exfoliated MoS_2. *Nano Lett.* **2011**, *11*, 5111−5116.

(15) Gomez, A. C.; Leeuwen, R.; Buscema, M.; Zant, H. S. J.; Steele, G. A.; Venstra, W. J. Single-layer MoS_2 Mechanical Resonator. *Adv. Mater.* **2013**, *25*, 6719−23.
(16) Tongay, S.; Zhou, J.; Ataca, C.; Lo, K.; Matthews, T. S.; Li, J.; Grossman, J. C.; Wu, J. Thermally Driven Crossover from Indirect toward Direct Bandgap in 2D Semiconductors: $MoSe_2$ and MoS_2. *Nano Lett.* **2012**, *12*, 5576−80.
(17) He, Q.; Zeng, Z.; Yin, Z.; Li, H.; Wu, S.; Huang, X.; Zhang, H. Fabrication of Flexible MoS_2 Thin-Film Transistor Arrays for Practical Gas-Sensing Applications. *Small* **2012**, *8*, 2994−99.
(18) Powell, M. J. The physics of amorphous-silicon thin-film transistors. *IEEE Trans. Electron Devices* **1989**, *36*, 2753−63.
(19) Nathan, A.; Kumar, A.; Sakariya, K.; Servati, P.; Sambadan, S.; Striakhilev, D. Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic. *IEEE J. Solid-State Circuits* **2004**, *39*, 1477−86.
(20) Klauk, H. Organic Thin Film Transistor. *Chem. Soc. Rev.* **2010**, *39*, 2643−2666.
(21) Dimitrakopoulo, C. D.; Malenfant, P. R. L. Organic Thin Film Transistor for Large Area Electronics. *Adv. Mater.* **2002**, *14*, 99−117.
(22) Kamiya, T. Present status of amorphous InGaZnO thin-film transistors. *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305.
(23) Nomura, K.; Ohata, H.; Takagi, A.; Kamiya, T.; Hirano, M. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488−492.
(24) Street, R. A. Thin Film Transistors. *Adv. Mater.* **2009**, *21*, 2007−2022.
(25) Das, S.; Appenzeller, J. On the Importance of Bandgap Formation in Graphene for Analog Device Applications. *IEEE Trans. Nanotechnol.* **2011**, *10*, 1093−1098.
(26) Lundstrom, M. *Nanoscale Transistors: Device Physics, Modeling and Simulation*; Springer: New York, 2006.
(27) Datta, S. *Quantum Transport: Atom to Transistor*; Cambridge University Press: New York, 2005.
(28) Chen, Z.; Appenzeller, J. Mobility extraction and quantum capacitance impact in high performance graphene field-effect transistor devices. *IEEE Int. Electron Devices Meet.* **2008**.
(29) Xia, J.; Chen, F.; Li, J.; Tao, N. Measurement of the quantum capacitance of graphene. *Nat. Nanotechnol.* **2009**, *4*, 505−509.
(30) Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. High-performance thin-film transistors using semiconductor nanowires and nanoribbons. *Nature* **2003**, *425*, 274−278.
(31) Engel, M.; Small, J.; Steiner, M.; Freitag, M.; Green, A. A.; Hersem, M. C.; Avouris, P. Thin Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays. *ACS Nano* **2008**, *12*, 2445−2452.
(32) Das, S.; Appenzeller, J. Evaluating the Scalability of Multilayer MoS2 Field Effect Transistor. Device Research Conference (DRC), Notre Dame, IN, June 23−26, 2013; pp 153−154.
(33) Das, S.; Appenzeller, J. Where Does the Current Flow in Two-Dimensional Layered Systems? *Nano Lett.* **2013**, *13*, 3396−402.
(34) Das, S.; Appenzeller, J. Screening and interlayer coupling in multilayer MoS_2. *Phys. Status Solidi RRL* **2013**, *7*, 268−273.
(35) Das, S.; Prakash, A.; Salazar, R.; Appenzeller, J. Towards Low Power Electronics: Tunneling Phenomena in TMDs. *ACS Nano* **2014**, *8*, 1681−1689.
(36) Kumar, A.; Ahluwalia, P. K. Electronic structure of transition metal dichalcogenides monolayers from ab-initio theory: new direct band gap semiconductors. *Eur. Phys. J. B* **2012**, *85*, 186.
(37) Liu, L.; Kumar, B.; Ouyang, Y.; Guo, J. Performance Limits of Monolayer Transition Metal Dichalcogenides Transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 3042−3047.